STAC™ BENCHMARK COUNCIL

STAC® Summit

A meeting for trading technologists of all stripes, from CTOs and tech-savvy quants to hard-core developers and infrastructure engineers.

June 5, 2012

Doors open at 12:30pm / Meeting starts at 1:00pm
Meeting will be followed by a networking reception

Conference Center at UBS Tower
One North Wacker Drive
Chicago

Gold Sponsors:

AGENDA

Welcome and STAC Update [slides]

STAC will provide a brief update on Council activities and cover some highlights of the just-released analysis of the 2012 STAC Latency Monitoring and Time Synchronization Survey.

Peter Lankford, Founder & Director, Securities Technology Analysis Center. Peter has overseen STAC since its birth in 2006. Before that, Peter was SVP of Information Management Solutions at Reuters, where he led the $240M market data systems business. Peter's team led Reuters into the business of low-latency direct feeds and catalyzed the widespread adoption of Linux on Wall Street by making RMDS available on that platform. Prior to Reuters, Peter held management positions at Citibank, First Chicago Corp., and operating-system maker IGC. Peter has an MBA, Masters in International Relations, and Bachelors in Chemistry from the University of Chicago.

Platforms for research and backtesting

In liquid markets, tick-to-trade latency hogs the technology limelight. But another type of latency is also a key to competitiveness: the latency of developing and deploying new trading strategies. Trading firms are constantly pushing to enable more rapid experimentation and adaption of algorithms to market conditions. Depending on how quants and developers tackle this issue, big bottlenecks can arise in compute, I/O, or programmer productivity. Niall will provide a customer perspective on the tradeoffs of various approaches. What's the best approach for moving from batch to near real-time analysis? For overall throughput and productivity, how best should we scale out the workloads? Where are the bottlenecks and what can we do about them? Can we believe the results we get?

Niall Dalton. [slides] Niall is an expert in algorithms and technology for low-latency, data-intensive systems in applications such as high-frequency trading. His 17 years of experience include working as Director of High-Frequency Trading at a Wall Street firm; as CTO of Kx Systems, a leading vendor of high-performance column-oriented database software widely used on Wall Street; as senior software engineer at NVIDIA; and as CTO at X.R.N.D, a European vendor of high performance parallel data analysis software. He has enjoyed a variety of engineering and research positions in Europe and the US in areas such as language design and compilers for parallel computing, data-intensive distributed systems and non-traditional database internals. He currently serves on the advisory board of MemSQL, creators of a realtime in-memory MySQL compatible database, and Calxeda, designers of a ultra-low power processors for hyperscale servers. Despite many publications and multiple degrees in Computer Science, Niall acquired the skills to swear fluently at multifarious hardware and software systems in a wide variety of common and obscure programming languages. He has never met an abstraction layer he didn't enjoy violating.

Technical Briefing: Opening up the I/O bottleneck in backtesting

DDN will discuss how leading trading firms are using storage architectures from the HPC world to enable breakthrough performance for strategy research and backtesting, and how such architectures work when based on DDN products.

Bob Gaines, Senior Sales Director, DataDirect Networks. [slides] Bob Gaines is senior director for DataDirect Networks solutions team for the US and Canada. He is a long-term veteran of the storage industry having spent the past 12 years at StorageTek, Sun Microsystems, and Oracle. He created StorageTek's state, local, & education sales practice that become Sun's government education and healthcare vertical via acquisition. Bob developed large-scale data management and storage architectures for government agencies and educational research labs.

Innovation Roundup – Round 1	
• "Accelerating Fast Workloads throughout the Front, Middle and Back Office" **[slides]**	**Bill Romano**, Senior Systems Engineer, Solace Systems
• "Scalable Low Latency Infrastructure" **[slides]**	**Amir Halfon,** Senior Director, Capital Markets, Oracle
• "Detecting Memory Errors, Leaks and Concurrency Violations in Kernel Modules and C/C++ Applications with Deterministic Precision and Zero False Positives" **[slides]**	**Himanshu Shukla**, CTO, Parallocity
• "The Power of Real Time Monitoring With MemSQL" **[slides]**	**Eric Frenkiel,** CEO, MemSQL

Technical Briefing: Sandy Bridge Performance

Intel and STAC (Peter Lankford, see above) will review recent research on optimizing both tick-to-trade and analytic workloads on Sandy Bridge and other platforms.

David O'Shea, Financial Services ISV Segment Manager, Intel. **[slides]** David has been with Intel for more than 15 years, the last 10 of which he has served as Intel's ISV lead within financial services. During that time, Intel platforms matured from file and print applications to the mission critical work horse of the industry. David has pioneered Intel's efforts to meet industry requirements for risk management, market data, and high frequency trading. Prior to Intel, David worked with leading software providers on RISC and PC platforms. David is married, has three children, and is an avid golfer with a high handicap.

COFFEE BREAK

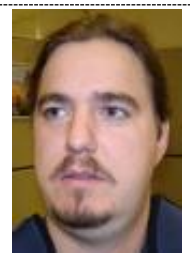
Innovation Roundup – Round 2	
• "Accessible Analytics - Building on CorvilNet" **[slides]**	**Raymond Russell,** CTO, Corvil
• "Low Latency to High IOPS: Wire to Storage Solutions" **[slides]**	**Brian Grant,** Sr. Systems Engineer, Emulex
• "Paradigm Shift: Accelerating Financial Applications Via The Programmable Network" **[slides]**	**Nick Ciarleglio,** System Engineer, Arista Networks
• "Cisco Innovations for High-Frequency Trading Workloads" **[slides]**	**Will Ochandarena,** Product Manager, Server Access & Virtualization Technology**,** Cisco

Not Your Father's Network

The network landscape is changing rapidly. Innovations in latency, scalability, and even programmability are redefining how we think about both switches and host interfaces. Our panelists will discuss what this means for trading firms and what we can expect leading trading architectures to look like a year from now.

Glenn Dasmalchi, Enterprise Sector CTO, Juniper Networks. Glenn is responsible for driving Juniper's Enterprise technology vision and related go-to-market strategy and execution globally. A proven technologist with many years of experience in the networking industry, he leads the integration of Juniper's end-to-end Enterprise architectures in the areas of Cloud, Data Center, Security, and Campus. Before joining Juniper, Glenn was Technical Chief of Staff in the Office of the CTO at Cisco, where he was responsible for identifying and developing strategy around technology-based market disruptions. He also served in several engineering leadership roles driving architecture and engineering development on switching platforms, including the Catalyst 6000 and Nexus 7000. Prior to the networking industry, Glenn co-founded Media Engineering, a technology consulting firm. He also served in a variety of leadership and engineering roles in several Silicon Valley startups and corporations, including HP, Apple, FirePower Systems, and Chelsio. Glenn holds BS and MS degrees in Electrical Engineering from Stanford.

Will Ochandarena, Product Manager, Server Access & Virtualization Technology, Cisco. Will is a Product Manager for Cisco's Nexus 3000 series switches, focusing on low latency switching for the Financial Services vertical. Prior to this position, Will spent five years in various roles within Cisco, including support and engineering for ethernet switching products. Will holds a BS in Computer Engineering from Rensselaer Polytechnic Institute and an MBA from Santa Clara University.



Doron Arad, Client Solutions Director, Mellanox Technologies. Doron has served as Mellanox's Client Solutions Director since February 2011. Previously, he served as Senior Solutions Architect at Voltaire from February 2007 to February 2011. From February 2002 to January 2007, Doron served as Data Center Manager at eBay. Doron holds a Bachelor of Science in Computer Science and Economics from Tel Aviv University and a Master of Business Administration with a concentration in marketing and Public Relations from Fairleigh Dickinson University.

Nick Ciarleglio, FSI Product Manager, Systems Engineer, Arista. Nick arrived at Arista Networks in 2008 as the company's first Systems Engineer. In his current role, Nick is responsible for network architecture consulting in the financial services vertical, and has specifically focused on end to end low-latency architectures. Nick also provides field feedback and "real world" expertise to the Arista development teams. Prior to his arrival at Arista, Nick was a Senior Technical Consultant for Hewlett Packard.

Accelerator Boards: Making Hardware Softer or Software Harder?

***Moderator*: Niall Dalton** (see first page)

FPGAs and more recently, network processors (NPUs), have secured a place in many low-latency trading shops. While most early adopters bought complete, integrated solutions from vendors, today many trading firms are going directly to component vendors and doing the integration themselves. These accelerators are effectively "bumps in the wire" that perform critical tasks directly within a network card or switch without needing to up-call a host system. What is the state of the art in these components? What differentiates them from each other? How broad a part can they play in the trader's arsenal? Just how tough are they to program, and how risky is it to slow down code change in a world of rapidly evolving requirements? How do the underlying technology roadmaps compare to those for CPU-based platforms?

Bruce Tolley, Vice President of Marketing, Solarflare. [slides] Bruce is responsible for solutions and technical marketing at Solarflare. Prior to joining Solarflare, Tolley was a Senior Product Line Manager at Cisco Systems where he launched Layer 2/3/4, Metro Ethernet and 10 Gigabit switching. Formerly Study Group Chair of the IEEE 802.3aq 10GBASE-LRM standards project, Tolley has been a frequent contributor to the IEEE 802.3 Ethernet standards projects and a frequent speaker at industry events such as IEEE 802.3 Working Group and Interop. He holds an MBA from Haas School of Business, UC Berkeley and a PhD from Stanford University.

Matthew Knight, President, Accensus. [slides] Matthew has been with Accensus for just over a year in the role of President. In that time, he has shaped their recently released new hybrid FPGA/CPU platform and overseen its introduction to market. Prior to Accensus, Matthew was with DRW Trading in Chicago, running technology research and development for the high-frequency and algorithmic trading desks. Before that he spent two blissful years at STAC focusing on measuring latency and designing and implementing benchmarks. Nine years at Reuters working mainly in the Market Data System realm and two years at BNP Paribas preceded that. Matthew's key expertise is in low-latency computing and networking across the whole stack.

Mohammad Darwish, Founder and CEO, AdvancedIO. [slides] A 20-year veteran of business and technology innovation, Mohammad leads AdvancedIO Systems, a company providing programmable Ethernet cards built for real-time performance in the financial and defense markets. AdvancedIO began leveraging 10GE and FPGA in 2004, beating the general market by five years. Mohammad excels in design and innovation in the field of real-time systems with focus on FPGA technologies. He has developed real-time software and defined radio products at Spectrum Signal Processing and digital image quality processors at Ward Labs. He took his expertise into the classroom, teaching senior classes at the University of British Columbia (UBC) and has been published in prestigious conferences on VLSI and parallel systems. He has a BSc in Computer Engineering and a MASc in Electrical and Computer Engineering from UBC, specializing in high-speed digital design.

Kelly Masood, President/CTO, Intilop. [slides] Kellly has over 27 years of hands-on development and management experience with many of the well-respected high-tech companies in Silicon Valley including: Burroughs, Unisys, Ford Aerospace, Loral/Lockheed Martin, NEC, Fujitsu, Network Peripherals, Silicon Graphics, Niksun. He founded Intilop in August 2004. Kelly has a BS/MS degree in Electrical Engineering from Texas A&M University. He has granted patents with more than 16 claims and 2 filed patents with 33 claims. Kelly has presented and written articles and papers on numerous technology topics.

Innovation Roundup – Round 3

• "Performance Like No Other" [slides]	**Bill McLane,** Sr. Product Architect, Messaging, TIBCO
• "Innovations in High Performance Messaging" [slides]	**Bob van Valzah**, Product Specialist, Informatica
• "Optimizing ProLiant Gen8 Systems for Ultra Low Latency" [slides]	**Lee Fisher,** Worldwide FSI-HPC Solutions, HP
• "Delivering and verifying Sub microsecond time at the Linux application layer" [slides]	**Paul Skoog,** Product Marketing Manager, Symmetricom

COCKTAIL RECEPTION