STAC™ BENCHMARK COUNCIL

STAC® Technology Conference

November 2, 2011
Doors open: 9:00am
Meeting starts: 9:30am

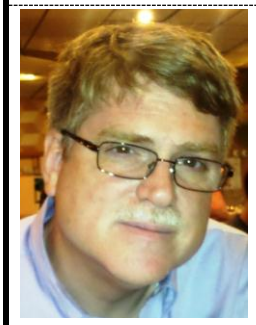
Bayards
Marine Room
One Hanover Square
New York, NY

Platinum Sponsors:

Gold Sponsors:

Standard Market Risk Technology Benchmarks [video/slides]

Lars will take attendees on a brisk walk through the market-risk suite of STAC-A2 Benchmarks.



Lars Ericson, Director, Citi. Currently working on WhatIf analytics for Citigroup's Cross Product Margining offering. Separately, assisting various analytics groups in Citi on parallelization with GPGPU to speed up current analytics. 22 years on Wall St. working on analytics for interest rates, munis, commodities, mortgages and convertible bonds. PhD in Computer Science from Courant Institute in correct program derivation using decidable sublanguages of set theory.

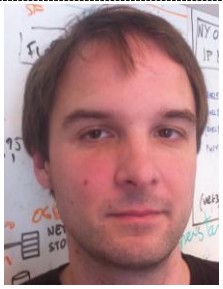
Issues in Computing Counterparty Risk [video/slides]

In this interactive session, Harvey will review the basic calculations involved in CVA and discuss the size of the compute challenge. He will then tackle questions such as: What is the proper way to perform CVA, and what are the dangers of taking shortcuts? What are the challenges in moving from single-security risk analysis to portfolio-level analysis? What are the technical implications of moving to intraday CVA? What are best practices for ensuring that the compute worklaod doesn't balloon out of control?

Harvey Stein, Head of Counterparty and Credit Risk, Bloomberg LP. Harvey graduated from Worcester Polytechnic Institute in 1982 with a Bachelor's degree in mathematics. After working at Bolt, Beranek and Newman for three years on developing and designing the precursor to the Internet, he went to graduate school at the University of California, Berkeley, where he studied arithmetical geometry while working at Wells Fargo Investment Advisors. Harvey received his PhD in mathematics from Berkeley in 1991. He's worked at Bloomberg for the last 18 years, where he built one of the top quantitative finance research and development groups in the industry. He's developed derivative securities valuation models for interest rate derivatives, mortgage backed securities, FX, credit, equities, and commodities, built Linux clusters to supply these valuations to Bloomberg's customers, and has published on the subject of derivative valuation, counterparty risk, and the impact of the financial crisis on mortgage valuation.

Breaking the Logjam in Credit and Counterparty Risk Management [video/slides]

Basel III and Dodd-Frank are driving banks to implement more rigorous credit and counterparty risk programs, including an increased focus on big data analytics. As a consequence, logjams occur due to contention for data and compute resources. Yet IT cannot simply add servers, storage, and networks in the current budget environment. Adam will detail some of the lessons that Platform Computing has learned about handling these logjams at its clients, including several of the world's largest investment banks.



Adam Vajda, Senior Systems Engineer/Architect, FSI, Platform Computing
Adam is a senior member of the Financial Services team at Platform Computing in New York. Over the past five years, he has focused on computational analytics and infrastructure in large Sell-side and Buy-side firms. He has co-authored papers in computational science and is well versed in a wide range of HPC technologies from compute grids to GPUs to data grids. Adam holds a degree in Computer Science and Astrophysics from the University of Western Ontario, Canada. In addition to technology, his interests include media, economics, and music.

COFFEE BREAK

Technical Brief: Intel's MIC (Many Integrated Core) Architecture [video/slides]

David will discuss the MIC architecture, a key part of Intel's strategy to bring increased performance with programmability to high-performance computing.

David O'Shea, Financial Services ISV Segment Manager, Intel. David has been with Intel for more than 15 years, the last 10 of which he has served as Intel's ISV lead within financial services. During that time, Intel platforms matured from file and print applications to the mission critical work horse of the industry. David has pioneered Intel's efforts to meet industry requirements for risk management, market data, and high frequency trading. Prior to Intel, David worked with leading software providers on RISC and PC platforms. David is married, has three children, and is an avid golfer with a high handicap.

Hadoop for Trading Firms: Beyond the Science Project [video/slides]

MapR has grabbed considerable attention as a new player on the Hadoop scene. From his cross-industry vantage point, Jack will discuss the kind of data problems for which Hadoop confers an advantage, as well as the cold realities of putting a Hadoop solution into production.

Jack Norris, VP Marketing, MapR. Jack has over 20 years of enterprise software marketing and product management experience in defining and delivering analytics, storage, and information delivery products. Jack began his career as a consultant with Andersen Consulting and Bain and Company.

Network Implications of Big Data Workloads [video/slides]

Will will discuss examples of Big Data deployments at Cisco customers to provide insight into key questions such as: How does the network impact performance of Big Data workloads? When does it make more sense to provision additional servers than to upgrade the network and vice versa?

Will Ochandarena, Product Manager, Cisco. Will is a product manager in Cisco's Server Access & Virtualization Business Unit, focusing on low latency switching in the financial vertical. Prior to this role, Will spent five years in various roles within Cisco, including support and engineering for Ethernet switching products. Will holds a BS in Computer Engineering from Rensselaer Polytechnic Institute and an MBA from Santa Clara University.

RAMcloud:Scalable High-Performance Storage Entirely in DRAM [video/slides]

RAMCloud is an open source project to deliver a new class of storage for datacenters where all data lives in DRAM at all times and large-scale systems are created by aggregating the main memories of thousands of commodity servers. According to John, RAMCloud combines low latency with large scale and uses disk or flash backups to provide durability and availability at least as good as today's disk-based storage systems.

John Ousterhout, Professor of Computer Science, Stanford University. John's current research focuses on infrastructure for Web applications and cloud computing. His prior positions include 14 years in industry where he founded two companies (Scriptics and Electric Cloud), preceded by 14 years as Professor of Computer Science at U.C. Berkeley. He is the creator of the Tcl scripting language and is also well known for his work in distributed operating systems and file systems. John received a BS in Physics from Yale and a PhD in Computer Science from Carnegie Mellon. He is a member of the National Academy of Engineering and has received numerous awards, including the ACM Software System Award, the ACM Grace Murray Hopper Award, the National Science Foundation Presidential Young Investigator Award, and the UC Berkeley Distinguished Teaching Award.

NETWORKING LUNCHEON

The STAC-M3 Effect [video/slides]

Peter Lankford, Founder & Director, STAC

Peter will review the STAC-M3 Benchmarks, the technology stacks that have been tested against them, and how they have provided an industry focal point for innovative performance engineering.

Peter Lankford, Founder & Director, Securities Technology Analysis Center. Peter has overseen STAC since its birth in 2006. Before that, Peter was SVP of Information Management Solutions at Reuters, where he led the $240M market data systems business. Peter's team led Reuters into the business of low-latency direct feeds and catalyzed the widespread adoption of Linux on Wall Street by making RMDS available on that platform. Prior to Reuters, Peter held management positions at Citibank, First Chicago Corp., and operating-system maker IGC. Peter has an MBA, Masters in International Relations, and Bachelors in Chemistry from the University of Chicago.

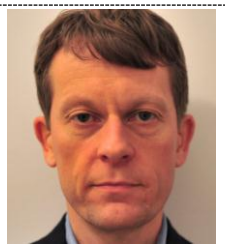
Innovation Roundup – Round 1

• "Scalability and Speed: Proof That You Can Have Both" [video/slides]	**Larry Jones,** Sr. Director, HPC and Life Sciences, DataDirect Networks
• "Spinning Rust is Dead" [video/slides]	**Cameron Campbell**, Director of Business Development, ION Computer
• "Kove DRAM Storage: The (STAC) Results Are In" [video/slides]	**John Overton, Ph.D.,** CEO, Kove

Panel: The New Frontier in Storage Performance [video]

It is well known that while storage capacity has met or exceeded advances in CPU and memory over the past few decades, storage performance has lagged them all by a few orders of magnitude. For trading organizations, storage performance is the gating factor on many important top-line activities such as strategy back-testing and risk management. However, recent innovations such as solid-state media (including flash and DRAM), higher speed interconnects, more powerful controllers, and smarter software may be opening up that bottleneck. Just how good are these new solutions, and what opportunities do they present?

Larry Jones, Sr. Director, HPC and Life Sciences, DataDirect Networks. Larry is charged with developing and evangelizing compelling storage solutions for the HPC, Finance and Life Sciences end markets. He has 30+ years experience in networking, storage, and technical marketing related to the cloud storage, financial services, telecommunications, collaboration software and High Performance Computing industries. Prior to his role at DataDirect Networks, Larry led the definition and introduction of the first parallel, object-based file system at Panasas, and held senior marketing roles at E*Trade, IBM, and Nortel Networks. Larry holds a BA in History from the University of Michigan, regularly contributes to trade journals, and has been a featured presenter at industry conferences.



John Overton, Ph.D. CEO, Kove. John founded Kove in 2004. Before that, John was founder and CTO of a company that built the fastest network-optimized database in the world. John has degrees from the University of Richmond, Harvard, and University of Chicago.

Keith Josephson, CTO, Ion Computer. Keith is co-founder and Vice President of Engineering for ION Computer Systems. He is the chief architect of ION's performance-oriented server and storage server products. Keith has led the development of ION's products for HPC customers and storage virtualization OEMs. Keith has 25 years of experience with server design and optimization, including storage sub-systems, Linux and real-time operating systems. Prior to joining ION, Keith held field engineering positions with Pioneer-Standard and Intel.

Innovation Roundup – Round 2	
• "Big Data/Big Compute" **[video/slides]**	**Ashwin Kohli**, Systems Engineer, Arista Networks
• "Squashing bugs: Innovative techniques for parallel code" **[video/slides]**	**Stephane Raynaud**, Principal Sales Engineer, Rogue Wave Software

Breakout Session: STAC Bi-Temporal Data SIG

Pearl Room

***** End users only *****

Technical Brief: Intel's Next-Gen Instructions - AVX, AVX2, and FMA [video/slides]

Mark will highlight key points from Intel's next-gen instruction sets. Click here for background documents.

Mark Davis, Senior Principal Engineer, Intel. Mark has been at Intel since 2001 In the Technical Computing, Analyzers, and Runtimes team, Mark designs and implements software-development tools for parallelism. Previously, he was architect and co-manager of Intel's Itanium Compiler Development team, providing high quality, high performance compilers for enterprise-class Itanium platforms. In his career, Mark has specialized in compiler optimizations, language design (Ada), performance analysis, and architecture. He earned his Ph.D. in Computer Science from Harvard University.

Technical Brief: Identifying Kernel Mode Data Races [video/slides]

High-performance systems in the financial services industry often require customizations to operating system kernels, device drivers, and third-party applications in order to gain the maximum possible efficiency and throughput. Whether these customizations are done in-house or through specialized vendors, quality tools for detecting concurrency errors, such as race conditions, atomicity violations, and data races, are necessary in order to gain the reliability required of financial services solutions. In some cases, even when the software is well-tested throughout the development lifecycle, these concurrency errors manifest themselves only when the full system is finally put together. And, when discovered, it can be inordinately difficult to communicate information about how to reproduce the error later. In this session, you'll learn how to identify kernel mode data races in your software at every phase of the application development lifecycle (development, test, and acceptance testing) and how to communicate errors you've identified back to the developers and vendors who may have caused them.

Peter Godman, Founder & CEO, Corensic. Peter joined Corensic from Isilon Sytems where, as Director of Software Engineering, he led development of several major releases of Isilon's award-winning OneFS distributed filesystem and developed around twenty patent-pending technologies. Prior to his six year tenure at Isilon, Peter led development of several generations of Linux-based client software at RealNetworks.

COFFEE BREAK

STAC Update [video/slides]

Peter Lankford, STAC

Peter will briefly review activity in a number of the STAC Benchmark™ domains.

Technical Brief: Automated Testing of RMDS [video/slides]

Peter Lankford, STAC

Recent market volatility and the resulting surge in data volumes have brought renewed focus to performance testing of critical enterprise systems like RMDS. Leading banks view performance testing as an essential part of their change-control process, whether the change is a new load of software or just a tweak to a buffer setting. Those tests must be comprehensive, disciplined, and scalable. And in today's headcount environment—where everyone is expected to do more with less—those tests must be automated. Peter will describe how leading banks perform rigorous, lights-out testing with the STAC-M2 Advanced Test Harness.

Innovation Roundup – Round 3

• "FSI-HPC: 5 HP updates in 5 minutes" [video/slides]	**Chris Ferrari**, HP Solution Architect, HP
• "TIBCO FTL® Goes Global" [video/slides]	**John Page**, Director of Business Development, Messaging, TIBCO Software
• "Need for Speed: Taming Latency" [video/slides]	**Raja Daita,** Chief Product Officer, SR Labs

STAC Network API Study A [video/slides]

Peter Lankford, STAC

Development groups creating low-latency applications often face network API choices. Anecdotes suggest that most trading apps still use the Berkeley Sockets API for communication, while a smaller number use RDMA. Some may use another OFED API: RDS. What are the pros and cons of these APIs and the multiple implementations now available for each? Key questions surround their performance, complexity, and resource usage, including the tradeoffs inherent in different usage patterns. STAC has recently performed research ("STAC Network API Study A") into these questions, with support from key networking vendors and the RDMA experts at the University of New Hampshire. This study is expected to be the first round of an interactive research program involving Council members. While the reports from Study A are reserved for premium STAC subscribers, Peter will provide highlights and discuss the contours of this ongoing research program.

Innovation Roundup – Round 4

• "Cisco Innovations for High Frequency Trading" [video/slides]	**Will Ochandarena,** Product Manager, Cisco
• "Implementation experience and performance results with the Solarflare 10GbE precision time network adapter" [video/slides]	**Bruce Tolley,** VP, Solutions Marketing, SolarFlare
• "Timekeeping Accuracy on Servers Under Load" [video/slides]	**Paul Skoog**, Product Marketing Manager, Symmetricom

Panel:
Time Sync for Our Time [video]

Notwithstanding predictions to the contrary, the latency race has not run out. Latency tolerances continue to drop by an order of magnitude every 2 to 3 years. How is this affecting time-sync strategies at trading firms? What about the cost of implementations? Do firms have a good grip on the pros and cons of different approaches? What are the best approaches? Our panel will debate.

Paul Skoog, Product Marketing Manager, Symmetricom. Paul Skoog has diverse experience in the engineering software and GPS positioning & timing markets. Current responsibilities include product management for GPS referenced network time servers and bus level timing products. Prior to joining Symmetricom, Paul was product manager for precision GPS positioning instruments for Trimble. He has also held engineering and product management positions in the dynamic signal analysis software market. Paul holds a BSME degree from California Polytechnic State University and an MBA from Santa Clara University Graduate School of Business..

Bruce Tolley, VP Solutions Marketing, Solarflare. Bruce is responsible for solutions and technical marketing at Solarflare. Prior to joining Solarflare, Tolley was a Senior Product Line Manager at Cisco Systems where he launched Layer 2/3/4, Metro Ethernet and 10 Gigabit switching. Formerly Study Group Chair of the IEEE 802.3aq 10GBASE-LRM standards project, Tolley has been a frequent contributor to the IEEE 802.3 Ethernet standards projects and a frequent speaker at industry events such as IEEE 802.3 Working Group and Interop. He holds an MBA from Haas School of Business, UC Berkeley and a PhD from Stanford University.

Will Ochandarena, Product Manager, Cisco. Will is a product manager in Cisco's Server Access & Virtualization Business Unit, focusing on low latency switching in the financial vertical. Prior to this role, Will spent five years in various roles within Cisco, including support and engineering for Ethernet switching products. Will holds a BS in Computer Engineering from Rensselaer Polytechnic Institute and an MBA from Santa Clara University.

Innovation Roundup – Round 5

• "Latency: not just a number" [video/slides]	**Raymond Russell,** CTO & Co-Founder, Corvil

Panel: Latency Monitoring - Adult, Adolescent, or Infant? [video]

If there were a Gartner hype curve for latency monitoring products, where would we be on that curve today? What is the state of monitoring across the industry? Likewise, how are trading firms handling time sync now? What are the issues and opportunities as enhanced monitoring and time sync functionality get built into the network? Our panelists will consider the evidence and provide their forecasts.

Raymond Russell CTO & Co-Founder, Corvil. Raymond is one of Corvil's founders and co-inventor of its core technology. Since joining Corvil in 2000 as Chief Technology Officer, Raymond has played an instrumental role in building a strong product suite around the core Corvil technology. As CTO, Raymond is focused on driving continued advancement and fulfillment of Corvil's innovations with a focus on applications and infrastructure in capital markets.

Henry Young, CEO, TS-Associates. TS-Associates specialises in monitoring and analysis of networks, financial middleware products and electronic trading systems. With the TipOff network monitoring appliance and the Application Tap software instrumentation card, TS-Associates provides a complete range of precision instrumentation solutions capable of providing nanometric transparency into the latency dynamics of trading systems. Prior to setting up TS-Associates in 1999, Henry worked as an independent consultant with investment banks and exchanges across Europe, USA and more recently Asia, specialising in high performance front office and electronic trading technologies. Henry holds an MSc in Computing from Imperial College and a BSc in Physics & Electronics from Edinburgh University.

Nick Ciarleglio, System Engineer, Arista Networks. Nick arrived at Arista Networks in 2008 as the company's first System Engineer. In his current role, Nick is responsible for network architecture consulting in the financial services vertical, and he has specifically focused on end to end low-latency architectures. He also provides field feedback and "real world" expertise to the Arista development team. Prior to his arrival at Arista, Nick was a Senior Technical Consultant for Hewlett Packard.

COCKTAIL RECEPTION

Hanover Room