STAC™ BENCHMARK COUNCIL

STAC® Performance Summit

November 7, 2011

Doors open at 1:00pm / Meeting starts at 1:30pm
Meeting will be followed by cocktails

Andaz Hotel
40 Liverpool Street
Great Eastern Room
London

Gold Sponsors:

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AGENDA

Welcome and STAC Update [slides]

Peter will briefly review activity in a number of the STAC Benchmark™ domains.

Peter Lankford, Founder & Director, Securities Technology Analysis Center. Peter has overseen STAC since its birth in 2006. Before that, Peter was SVP of Information Management Solutions at Reuters, where he led the $240M market data systems business. Peter's team led Reuters into the business of low-latency direct feeds and catalyzed the widespread adoption of Linux on Wall Street by making RMDS available on that platform. Prior to Reuters, Peter held management positions at Citibank, First Chicago Corp., and operating-system maker IGC. Peter has an MBA, Masters in International Relations, and Bachelors in Chemistry from the University of Chicago.

Technical Brief: Automated Testing of RMDS [slides]
Peter Lankford, STAC

Recent market volatility and the resulting surge in data volumes have brought renewed focus to performance testing of critical enterprise systems like RMDS. Leading banks view performance testing as an essential part of their change-control process, whether the change is a new load of software or just a tweak to a buffer setting. Those tests must be comprehensive, disciplined, and scalable. And in today's headcount environment—where everyone is expected to do more with less—those tests must be automated. Peter will describe how leading banks perform rigorous, lights-out testing with the STAC-M2 Advanced Test Harness.

Innovation Roundup – Round 1

• "Informatica Ultra Messaging: Low Latency / Broad Functionality Across the Enterprise" [slides]	**Todd Montgomery**, VP Architecture, Messaging Business Unit, Informatica
• "TIBCO FTL® Goes Global" [slide]	**John Page**, Director of Business Development, TIBCO
• "FSI-HPC: 5 HP updates in 5 minutes" [slides]	**Steve Mayo**, HP Pre-Sales Consulting, HP
• "Cisco Innovations for High Frequency Trading" [slides]	**Yang Yang**, Technical Marketing Engineer, Cisco

STAC Network API Study A [slides]
Peter Lankford, STAC

Developers writing applications directly to a network interface have several choices. What are the pros and cons of APIs like Sockets, RDMA, and RDS and the implementations available for each? Key questions are their performance, complexity, and resource usage, including the tradeoffs of different usage patterns. STAC has recently researched these questions in "STAC Network API Study A," with support from key networking vendors and the RDMA experts at the University of New Hampshire. This study is expected to be the first round of an interactive research program involving Council members. While the reports are reserved for premium STAC subscribers, Peter will offer highlights and discuss this ongoing research program.

Technical Brief: Intel's Next-Gen Instructions - AVX, AVX2, and FMA [slides]

Evgueny will highlight key points from Intel's next-gen instruction sets. Click here for background documents.

Evgueny Khartchenko, Senior Software Application Engineer, Intel® DRD. Evgueny joined Intel 12 years ago with a background in Computation Fluid Dynamics. He initially joined Intel as a first line manager of VTune performance Analyzer development. From 2003 to 2007, Evgueny held consulting and technology management roles where he enabled EMEA and UK FSI Customers with Intel Tools and Intel technologies for High Performance Computing. Since 2007, Evgueny has been a technical lead at Intel's FasterLab. There he works with UK FSI customers on latency optimizations, developing latency analysis tools, and facilitating feedback to Intel's network group, processor architects and software tools development groups.

Innovation Roundup – Round 2

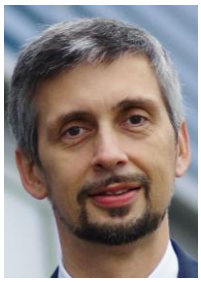
• "Squashing bugs; Innovative techniques for parallel code" [slides]	**Dean Stewart**, Senior Sales Engineer, Rogue Wave
• "How to Achieve Sub-Microsecond Synchronization Accuracy on Application Level" [slides]	**Nikolaus Kerö**, CEO, Oregano Systems
• "Implementation experience and performance results with the Solarflare 10GbE precision time network adapter" [slides]	**Dr David Riddoch**, Chief Software Architect, Solarflare
• "Timekeeping Accuracy on Servers Under Load" [slides]	**Paul Skoog**, Product Marketing Manager, Symmetricom
• "Why your traders are driving the demand for precision timing" [slides]	**Victor Yodaiken,** CEO, FSM Labs

Coffee Break

Panel: Time Sync for Our Time

Notwithstanding predictions to the contrary, the latency race has not run out. Latency tolerances continue to drop by an order of magnitude every 2 to 3 years. How is this affecting time-sync strategies at trading firms? Do firms have a good grip on the pros and cons of different approaches? What are the best approaches? Our panel will debate.

Paul Skoog, Product Marketing Manager, Symmetricom. Paul Skoog has diverse experience in the engineering software and GPS positioning & timing markets. Current responsibilities include product management for GPS referenced network time servers and bus level timing products. Prior to joining Symmetricom, Paul was product manager for precision GPS positioning instruments for Trimble. He has also held engineering and product management positions in the dynamic signal analysis software market. Paul holds a BSME degree from California Polytechnic State University and an MBA from Santa Clara University Graduate School of Business..



Nikolaus Kerö, CEO, Oregano Systems. After receiving a Masters Degree in Communication Engineering with distinction from the Vienna University of Technology, Nikolaus led the ASIC design division at the university's Institute of Industrial Electronics, successfully managing numerous research projects and industry collaborations. His research activities centered on distributed systems design, especially highly accurate and fault- tolerant clock synchroni-zation. In 2001 he co-founded Oregano Systems Design & Consulting Ltd. as a university spin-off. While offering embedded systems design services to customers, Oregano transferred research results into a complete product suite for highly accurate clock synchronization under the brand name syn1588®, for which Nikolaus manages both development and marketing. He is an active member of the IEEE1588 standardization committee and holds frequent seminars on clock synchronization for both industry and academia.

Victor Yodaiken, CEO, FSMLabs. Victor co-founded FSMLabs in 1999. since 2007, FSMLabs has developed software for the enterprise and financial trading markets. FSMLabs began as a developer of the RTLinux real-time operating system, used to control Jet Engine tests stands, robots, mobile phones, and software radios, among other products. RTLinux was sold to WindRiver Systems in 2007. Prior to founding FSMLabs, Victor worked in academia and as an industry consultant. He was a professor of Computer Science at New Mexico Tech, a Research Professor and Post-Doc at the University of Massachusetts (Amherst), a visiting lecturer at Beijing Aerospace University, a consultant on storage systems and financial software projects and a principal engineer of a fault-tolerant system startup. He has 4 US Patents.

David Riddoch, Chief Software Architect, Solarflare. David co-founded Level 5 Networks in July 2002 and joined Solarflare when it merged with Level 5 in April 2006. David is the architect and lead developer of Solarflare's market leading OpenOnload network acceleration middleware. David's mission is to deliver absolutely the best possible performance without asking users to abandon the standard network stack: Sockets, TCP, UDP and Ethernet.

Yang Yang, Technical Marketing Engineer, Cisco. Yang is responsible for driving technology adoption in Nexus access switch platforms. He works closely with the core engineering team, sales team, and third-party vendors to deliver innovative data center access switch platforms. He is a veteran of 11 years at Cisco, with solutions experience including routing, switching, multicast, and security. Currently he is focused on low-latency switching architecture, performance analysis, and monitoring, as well as driving the Precision Timing Protocol (PTP) implementation in the Nexus platform to provide sub-micro second accuracy timing solutions for HFT and data center networks.

Innovation Roundup – Round 3	
• "Latency: More Than Just a Number" **[slides]**	**Ken Jinks,** Product Manager, Corvil
• "Precision and Accuracy .... Faking Exposed ..." **[slides]**	**Rony Kay**, CEO, cPacket
• "Enhancing Network Instrumentation" **[slides]**	**John Peach**, Systems Engineer, Arista Networks

Panel: Latency Montioring: Adult, Adolescent, or Infant?

If there were a Gartner hype curve for latency monitoring products, where would we be on that curve today? What is the state of monitoring across the industry? What are the issues and opportunities as enhanced monitoring gets built into the network? Our panelists will consider the evidence and provide their forecasts.

Henry Young, CEO, TS-Associates. Henry founded TS-Associates, which specialises in monitoring and analysis of networks, financial middleware products and electronic trading systems. With the TipOff network monitoring appliance and the Application Tap software instrumentation card, TS-Associates provides a complete range of precision instrumentation solutions capable of providing nanometric transparency into the latency dynamics of trading systems. Prior to setting up TS-Associates in 1999, Henry worked as an independent consultant with investment banks and exchanges across Europe, USA and more recently Asia, specialising in high performance front office and electronic trading technologies. Henry holds an MSc in Computing from Imperial College and a BSc in Physics & Electronics from Edinburgh University.

Ken Jinks, Product Manager, Corvil. Ken has over 15 years' experience designing and creating products for the telecommunications and financial technology markets. He joined Corvil in September 2003 and has been in product management since the inception of the CorvilNet product. Ken works closely with all parties in the trading loop including venues, service providers, market makers and tier 1 investment banks to enable effective analysis of their high performance trading systems and products. He works with these customers, Corvil's sales and development teams, and industry experts to to drive the Corvil product roadmap to maximise value for existing and future Corvil customers. He previously worked in Alcatel/Newbridge Networks in both product development roles and sales engineering roles working with the largest telecommunication providers in the world. His career has included international assignments in Canada, UK, US and Ireland. Ken holds a degree in Electronic Engineering.

John Peach, Systems Engineer, Arista. John provides EMEA-wide technical consultancy for Arista Networks, the pioneer of next generation open networking platforms targeting high-value financial, HPC and Cloud data centre applications. With experience across telco, HPC and large enterprise networking through roles with several vendors, John's focus is on improving not only performance but also the manageability of infrastructure through instrumentation, automation and open systems.

Dr. Rony Kay, CEO, cPacket Networks. Rony combines unique expertise in high performance hardware-software design and algorithms. Rony founded cPacket Networks and is the chief architect of the company's hardware and software technology. Prior to this, Rony worked for Intel's Enterprise Platform Group, where he managed engineering teams working on multicore high-end server processors. Previously, he spent five years with IBM where he was a research fellow and a manager of cutting edge software and hardware development; he brought several innovations from inception, through concept-tual design and product development, to execution of successful customer deployments. Earlier he held positions in R&D, operations management, and IT optimization consulting. Rony is the author of multiple technical papers and eight patents. He earned his Ph.D. in Computer & Electrical Engineering from Carnegie Mellon University.

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