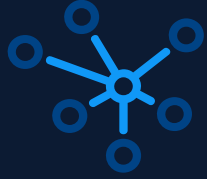




LMS
LIQUID-MARKETS SOLUTIONS

Transforming the Costs and Potential for Market Access

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Shōganai...

"It Cannot Be Helped"

Assuming & Accepting
A Less Than
Desirable Outcome.

October 17, 2020



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Shōganai
Prevents
The
Possible

Shōganai:

- **Limits** Progress
- **Overlooks** Innovation
- **Dismisses** Insight, Perspective & Need
- **Accepts** The Inefficient & Inappropriate



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The
Possible
Captures
Untapped
Opportunity

Why Accept Limitations?

When **Bottlenecks Can Be Eliminated**

Why Accept Total Transmit Latency of 1000s of ns¹?

When You Can Do It **All in 650ns¹**

Why Accept Compromise?

When a 360° **Plug & Play Solution Exists**

Why Pay \$100M PA to Provide Market Access?

When **\$50M Provides a Differentiated Service**

¹Not a STAC Benchmark



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Success
Is
Measured
By
Alpha

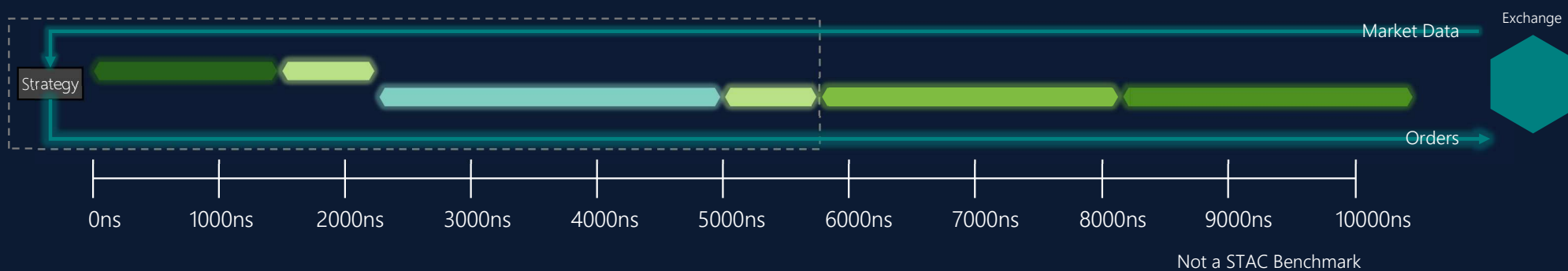
Alpha is Directly Correlated to Latency

What Matters is the Totality of Latency



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The Totality of Latency Exceeds 10,500ns



Components of Latency

Trading
Strategy Server

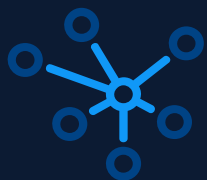
Kernel Bypass &
PCIe & Network Stack

Broker
Validation & Risk Checks

Trading
Validation & Risk Checks

Trading
Market Data Parsing

Exchange-Facing
Switch Functionality



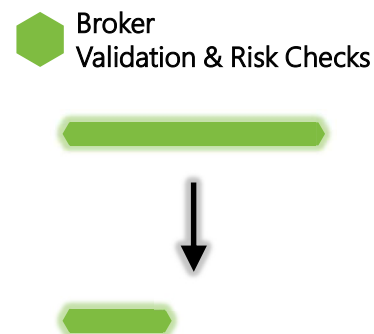
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Single-Point Solutions

Ignore

The Totality Of Latency

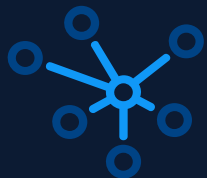
Marginal Gains - A Fraction of The Totality of Latency



...and the Remaining 9,000ns¹ Or So of Latency?

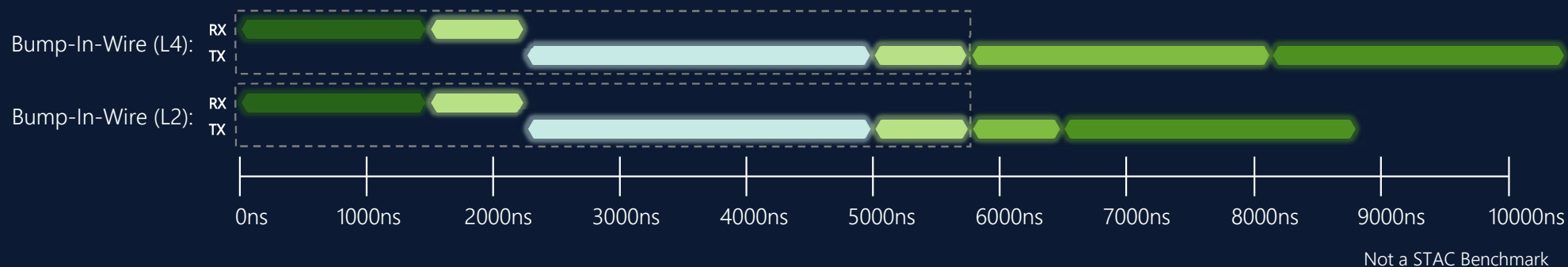
Shōganai?

¹Not a STAC Benchmark



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Investors Assume that Latency is Inevitable...



Components of Latency

Trading
Strategy Server

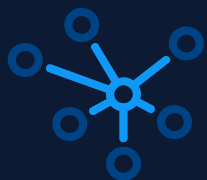
Kernel Bypass &
PCIe & Network Stack

Broker
Validation & Risk Checks

Trading
Validation & Risk Checks

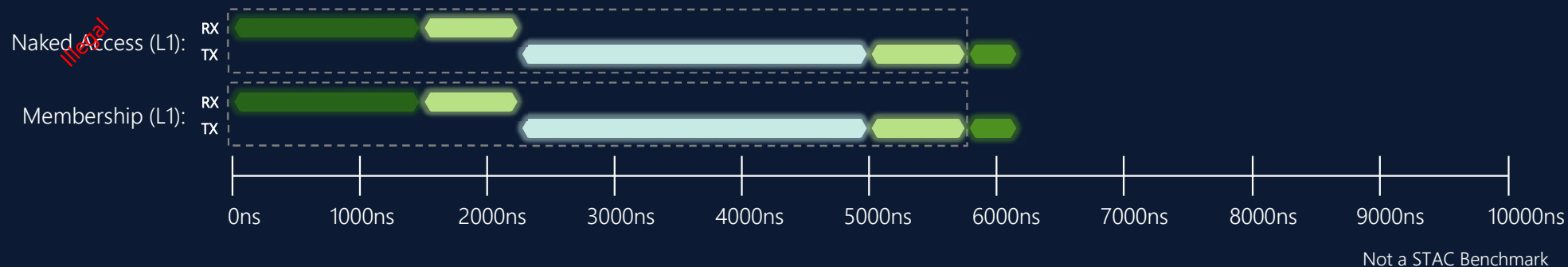
Trading
Market Data Parsing

Exchange-Facing
Switch Functionality



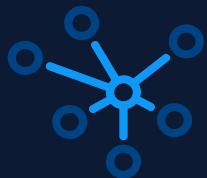
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...and Some Firms Create Marginal Improvements via Increased Risk...



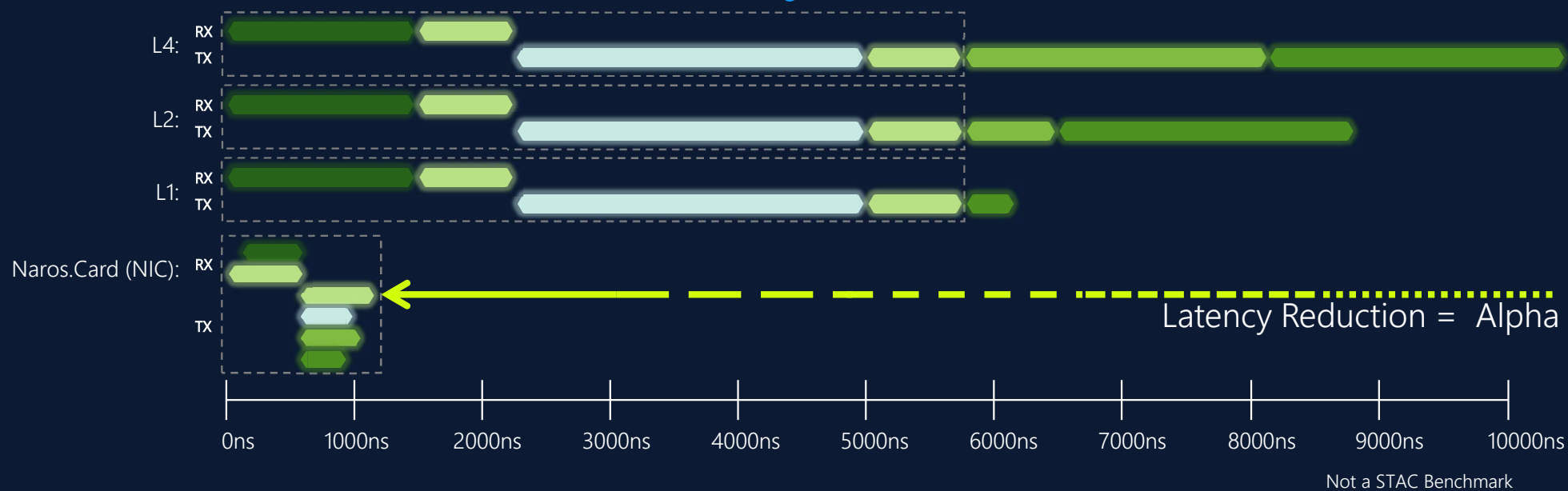
Components of Latency

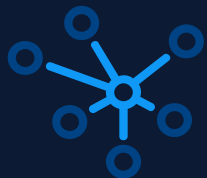




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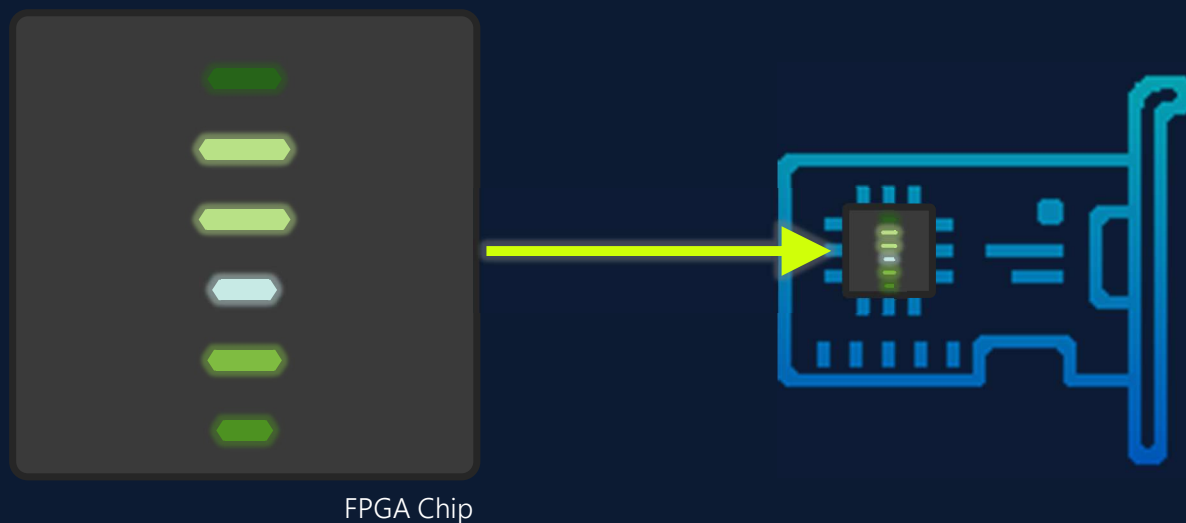
...LMS Rejects Status Quo...





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...LMS Embraces The Possible



- NIC w/Embedded FPGA
- Combined Functionality
- Complete Parallelization
- Encrypted Logic

Functional Components



OTP Register-Based
eFuse Encryption



Kernel Bypass &
PCIe & Network Stack



Broker
Validation & Risk Checks



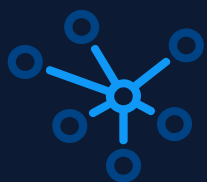
Trading
Validation & Risk Checks



Trading
Market Data Parsing



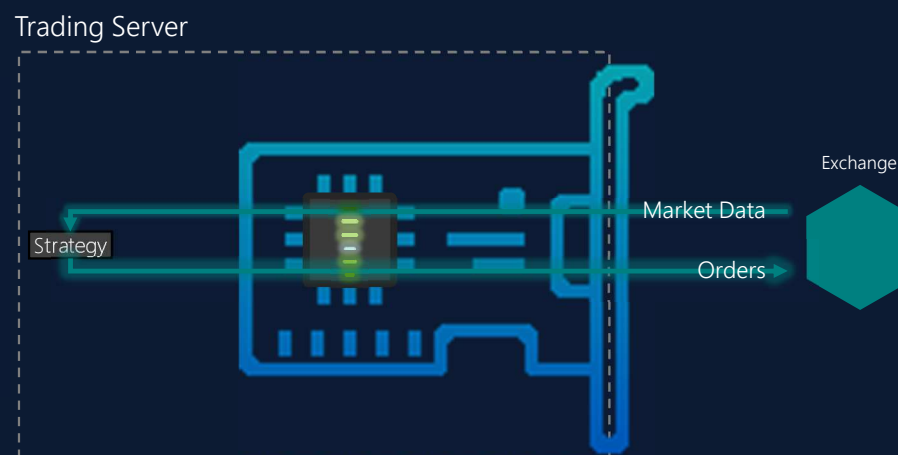
Exchange-Facing
Switch Functionality



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LMS Delivers The Possible

- Direct Venue Access
- Combined Functionality
- Unparalleled Performance



Functional Components



OTP Register-Based
eFuse Encryption



Kernel Bypass &
PCIe & Network Stack



Broker
Validation & Risk Checks



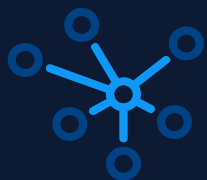
Trading
Validation & Risk Checks



Trading
Market Data Parsing



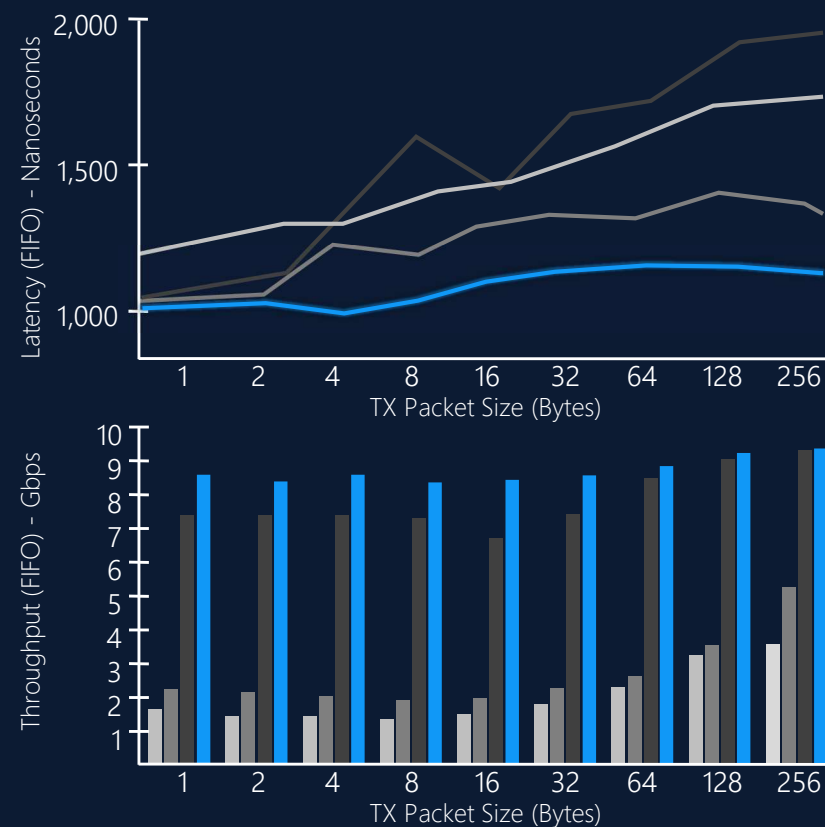
Exchange-Facing
Switch Functionality



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Naros.Card is Also The Most Performant NIC Available

- Unparalleled No-Compromise Low-Latency & Throughput
- Latency: Outperforms Other Solutions by 12% to 26%
- Throughput: Outperforms Other Solutions by 12% to 257%
- Consistent Performance Regardless of Message Size



Not a STAC Benchmark



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Solutions for Institutional Connectivity & Venue Access

Naros.Card



Designed and Optimized for Latency-Sensitive Trading

- Venue Access No Less Than 6x Faster Than Competitors
- Direct Venue Access w/Complete Regulatory Conformance

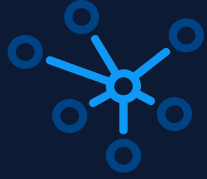
Naros.Hub



Designed and Optimized for Connectivity & Routing

- 667x Per-Device Capacity Advantage vs Traditional Server
- 2404x Annual kWh Cost Reduction vs Traditional Server

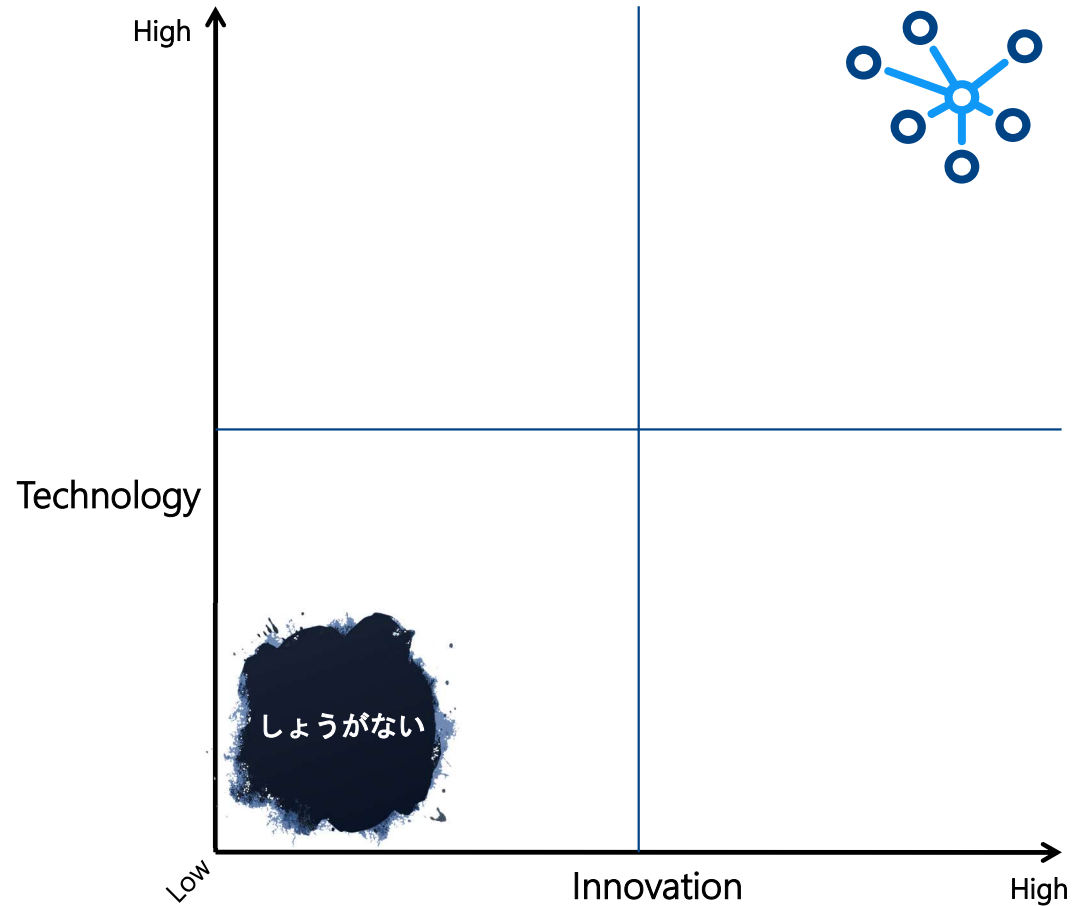
Proven Technology - Innovative FPGA Implementation w/US Patents 9,501,795 & 10,269,071; Others Pending



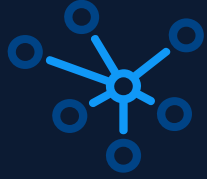
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LMS Delivers The Possible
Unparalleled Performance
Unique Yet Proven
Eliminates Compromise

October 17, 2020



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The Global Standard
Ultra-Low-Latency
&
Ultra-High-Capacity
Venue Access
&
Connectivity

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