Hacking the Packet in ASIC with an eFPGA

STAC Presentation, 11/1/2021

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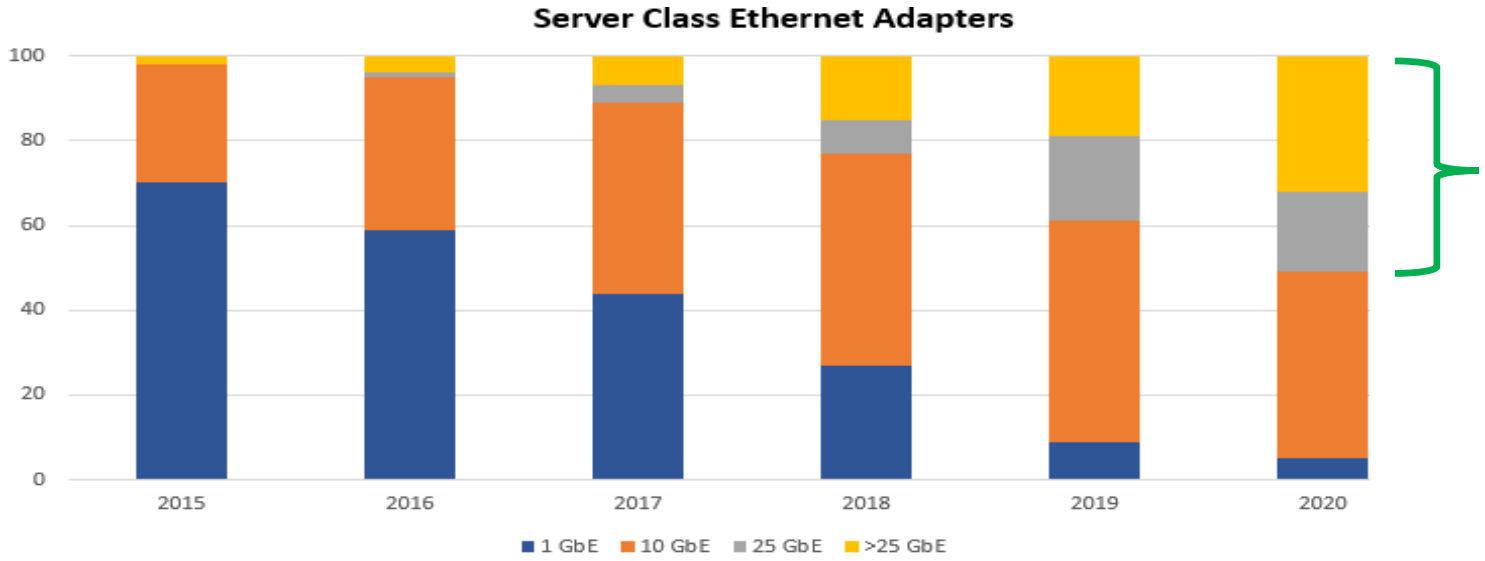
How to Achieve UDP-to-TCP loopback latency of under 10 ns with an eFPGA-enabled ASIC

Agenda:

1. SerDes support on next generation large package FPGAs
2. eFPGA overview and HFT benefits
3. Example HFT ultra-low-latency block diagram
4. Overview of the TSMC VCA program
5. Highlights of the Achronix eFPGA IP solution

Large Package, High-End FPGA Solutions Move to Support LR SerDes



Port speeds of 25 Gbps and above require forward error correction (FEC) to ensure interoperability

Forward Error Correction for 25G transceivers (IEEE 802.3by)

Fire-code FEC adds ~82 ns latency

FC-FEC (IEEE 802.3 clause 108)

Reed-Solomon FEC adds ~250 ns latency

RS-FEC (IEEE 802.3 clause 82)

EE Concerns for large-package, high-end FPGAs

- SerDes drive strength and insertion loss:
  - Drive meaningful PCB trace lengths
  - Avoid FPGA routing congestion close to the package
  - Provide support for connectors and backplanes

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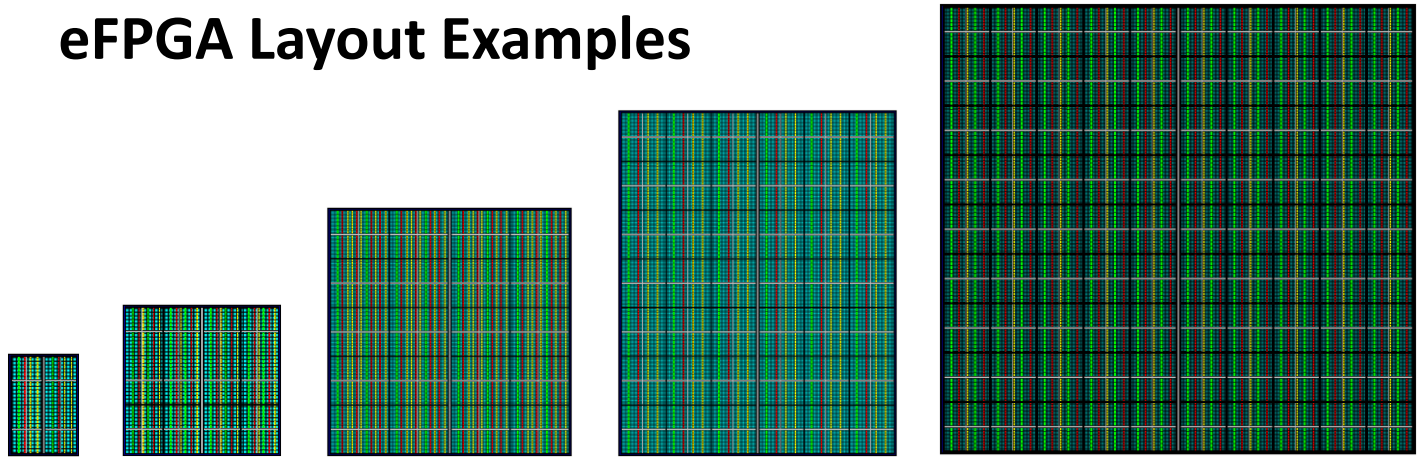
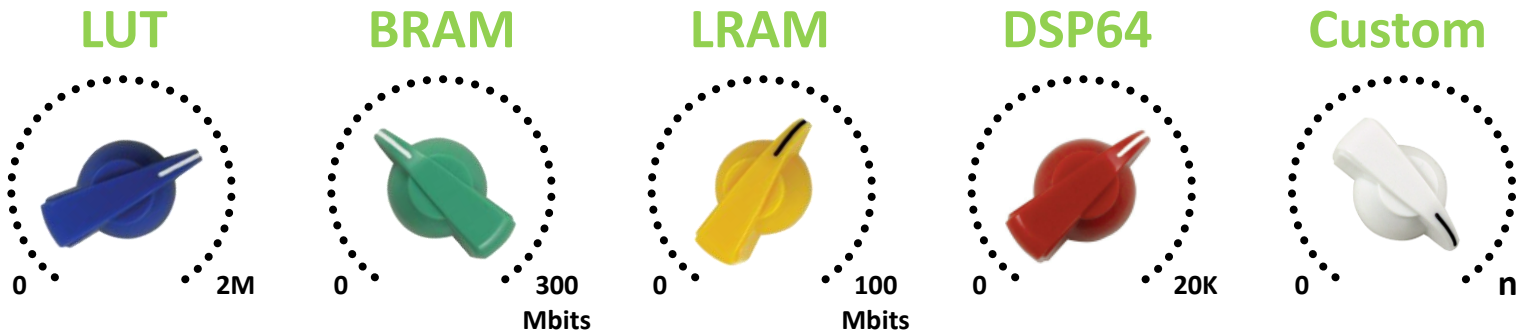
eFPGA Overview - Flexible Fabric Configuration and Sizing

- eFPGA resources are designed as building block structures that combine easily
- The customer defines an eFPGA resource mix to best meet their needs
- IP is delivered as a set of physically laid out transistors for efficient ASIC integration

eFPGA Layout Examples





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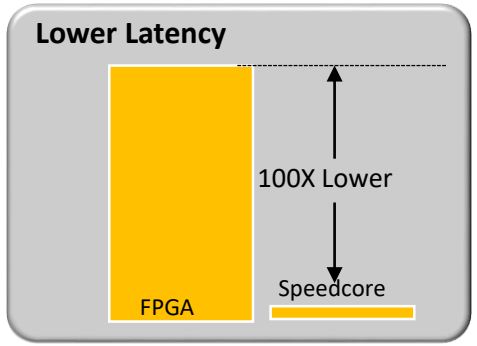
Top Three Benefits of an eFPGA-enabled ASIC for HFT

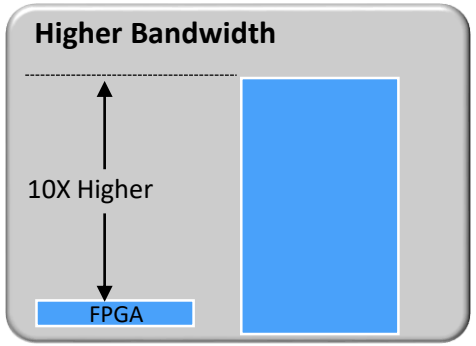
1. Enables a programmable tick-to-trade solution with best-in-class latency

2. Maintain your current technology flow with FPGA updates

3. Define your own custom architecture to get the most out of your trading platform



- **100x lower FPGA-to-ASIC latency**
- **Direct die connectivity**
- **Custom interconnect**



- **10x increase in bandwidth vs. standalone FPGA**
- **Direct die connectivity**

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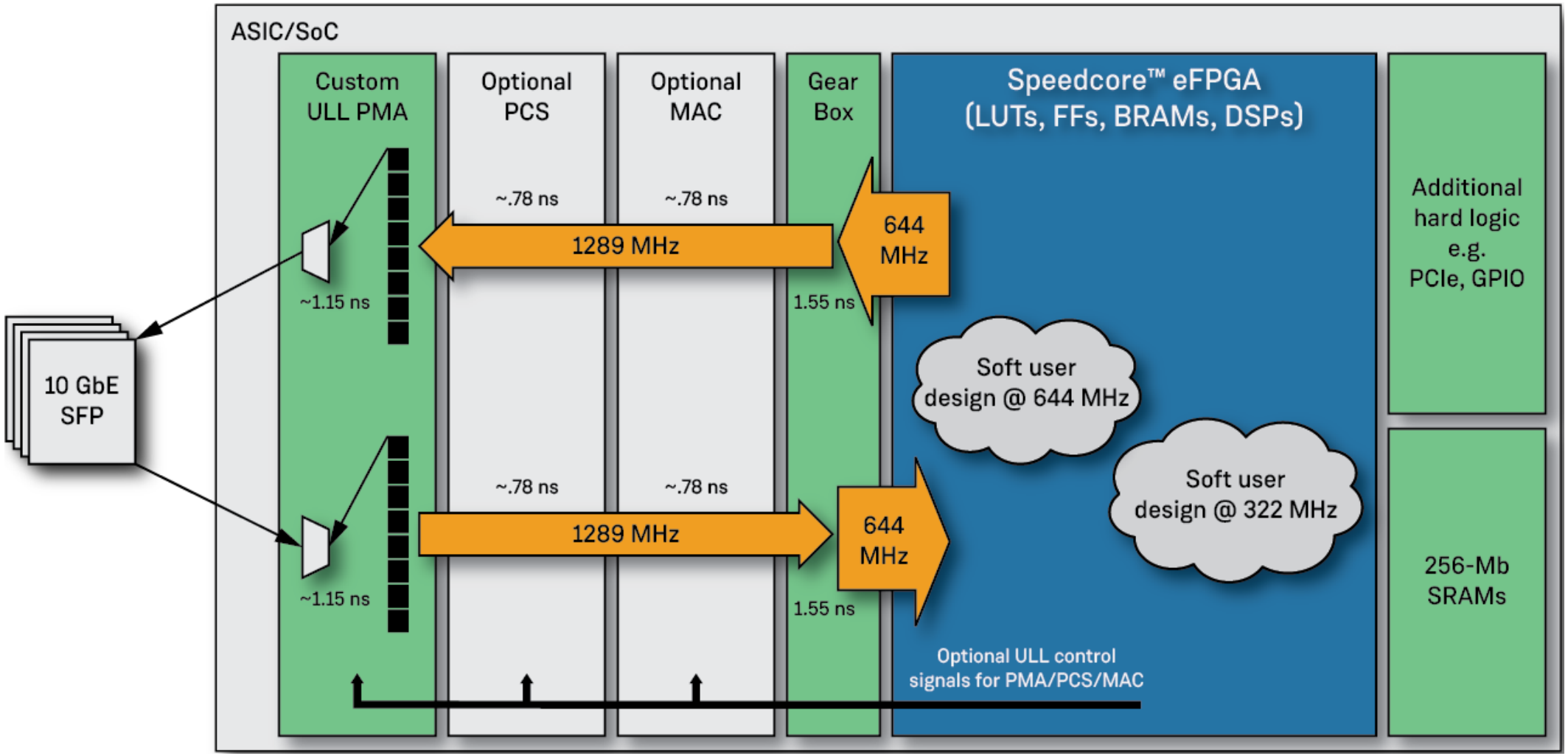
UDP-to-TCP Loopback Latency of Under 10 ns with a ULL Data Path



Not a STAC benchmark

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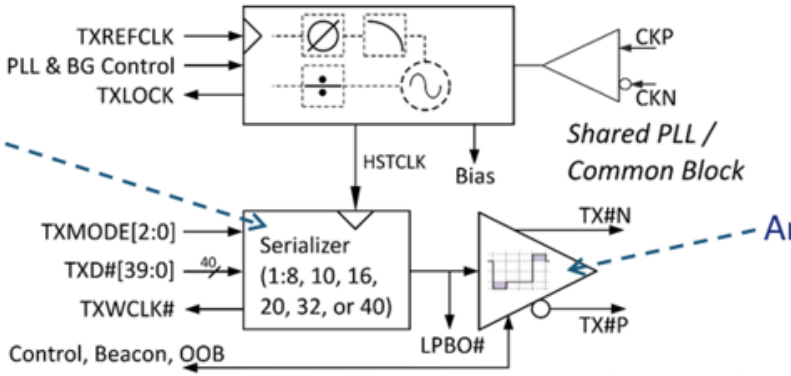
Hardware-Proven, Ultra-Low-Latency PMA

Low latency option

Silicon Creations

5 UI from rising edge of TXWCLK# to first bit out of Serializer

& Ser/Des width can be made 8b, 22b, to match FIFO…



Analog delay < 1 UI

Example with 10.3Gbps, 8b word. Loop back Latency = 2.23 ns

- Tx: 5 + 1 UI = 0.58ns
- Rx: 8 + 1 UI = 0.87ns
- Channel: 8 UI = 0.78ns

TSMC 12/16FFC supports to 16Gbps/lane; 25.8Gbps in planning

8 UI from last bit received to rising edge of RXWDCLK# (data ready)

Analog delay < 1 UI

DFE not normally used in low latency applications

Slide courtesy of Silicon Creations

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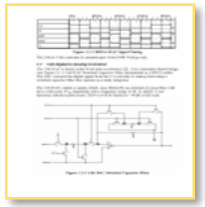
TSMC Value Chain Aggregators

- TSMC VCA program is well established and looking for new customers
- Thousand of successfully completed SoC and ASIC developments
- One-stop shop for ASIC design and manufacturing
- Support for low-volume, multi-project wafers as well as full wafer production

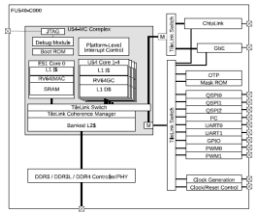
TSMC VCA Program

Specification



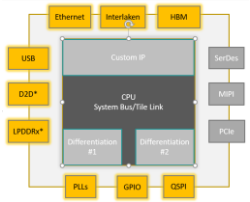
Product Requirement & Specification

Architecture



Architecture Analysis, RTL Design & Verification

IP



IP Development, Selection & Integration

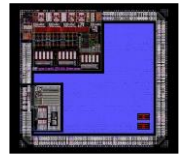
Software

Driver Development, Firmware, RISC-V Tool Chain

Prototyping

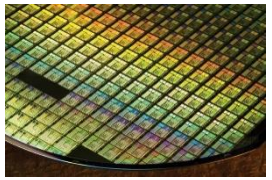
FPGA & Emulation

Physical Design



Physical Design

Fabrication



Wafer Fabrication

Flexible Engineering Relationships

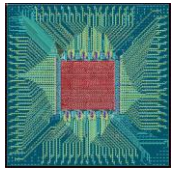
Spec Handoff ➔ Chip

RTL Handoff ➔ Chip

Netlist ➔ Chip

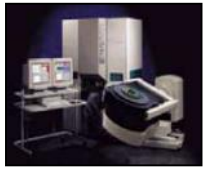
GDS2 Handoff ➔ Chip

Assembly



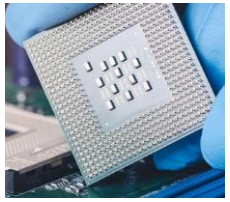
Package & Assembly

Test



Test & Product Engineering

Chips



Packaged ASIC Parts

Boards

Board Design & Manufacturing

Silicon Bring Up

Post Silicon Validation & Software Bring-up

Production

Production & Logistics

Achronix Speedcore™ eFPGA Compiler: Fast Development of Customer-Specific Speedcore IP

Inputs

Resource Mix

- LUT/register count
- Memory configuration
- Memory density
- DSP density
- Custom eFPGA tiles
- Number of I/O
- Aspect ratio

Technology Decisions

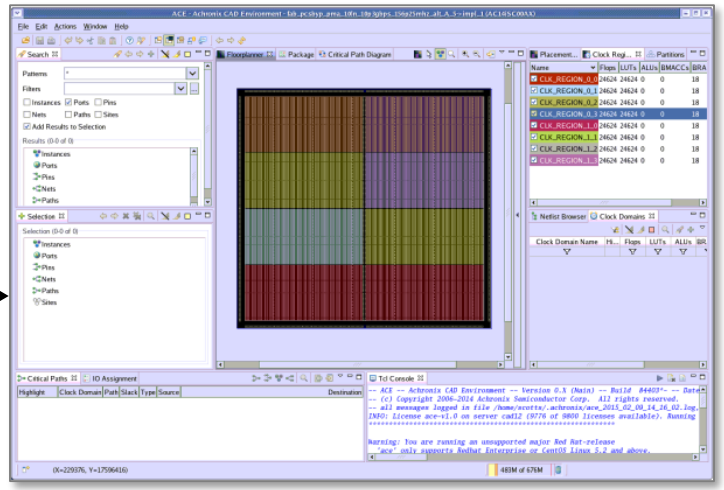
- Foundry
- Technology node
- Voltage
- Process node
- Metal stack

Deliverables

IP Deliverables

- GDSII of eFPGA IP core
- Simulation files
- SI and PI models
- Test models
- Timing
- Documentation

Custom ACE Design Tool Suite



Over 10 million Speedcore eFPGA IP cores have shipped in customer ASICs

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Thank You

Achronix is here to help you make your next eFPGA enabled ASIC a success!

We look forward to meeting you.
Please come to the Achronix Semiconductor breakout sessions to learn more about our Speedcore eFPGA technology.

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