Why Firms are Moving to ASIC and How the Process Works

Adam Sherer, Digital Verification Account Technical Executive, Cadence Design Systems

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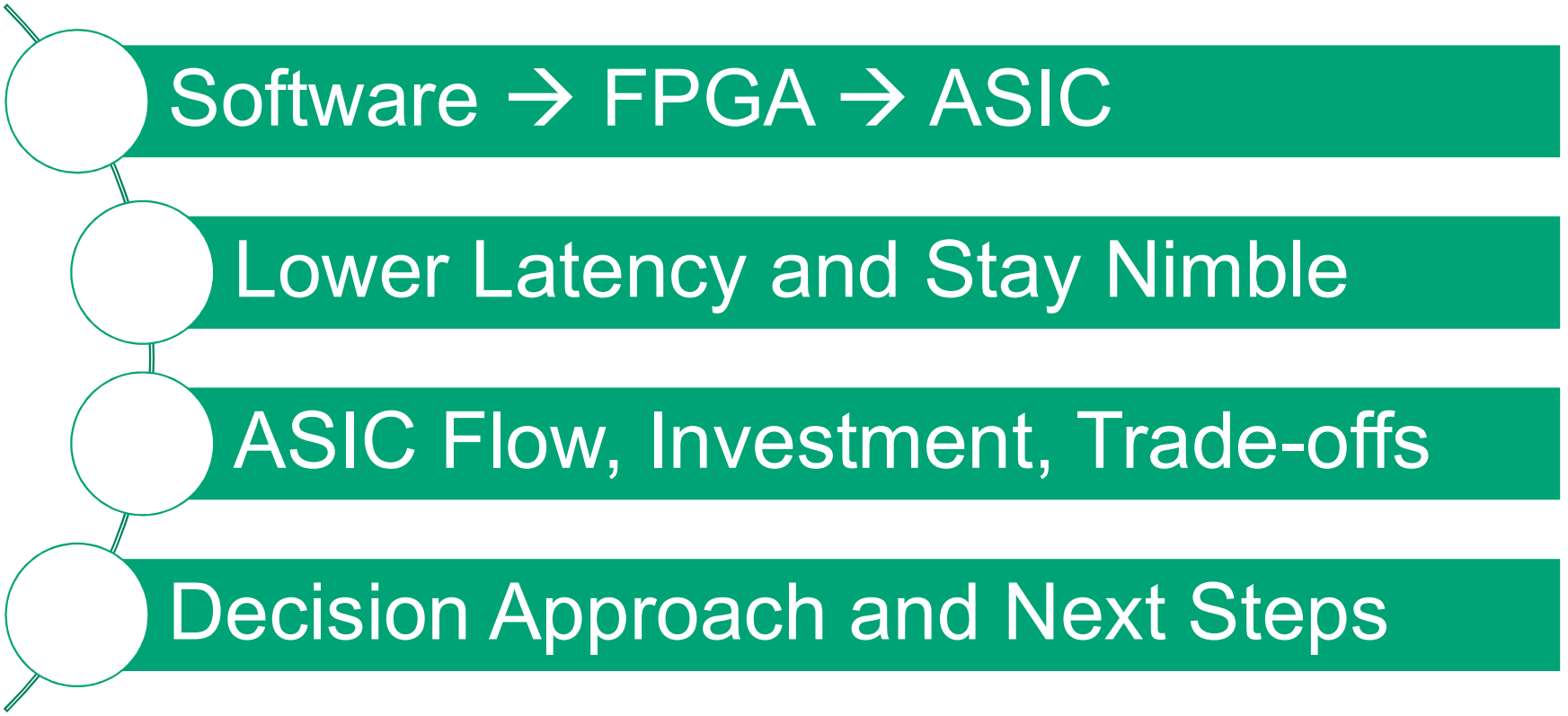
Agenda



Financial Analytics Evolution

ASIC to support faster ethernet and enable edge intelligence

HPC | Custom Drivers | ASIC Accelerator | Updateable Analytics

FPGA to reduce packet latency and enable edge computing

HPC | Custom Drivers | FPGA Accelerator

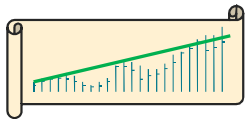
Driver SW to reduce packet latency

HPC | Custom Drivers

Financial SW / Big Data Analysis

High-Performance Compute (HPC)

Paper Charting



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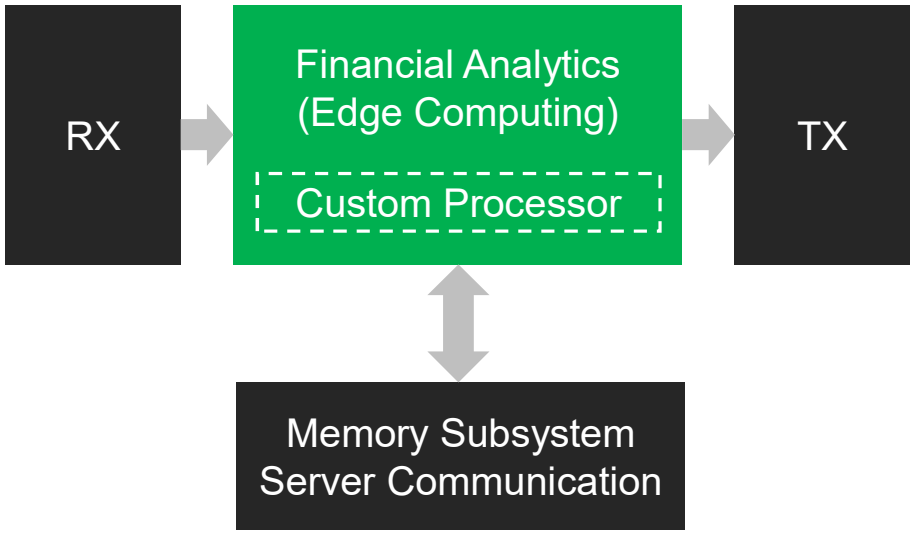
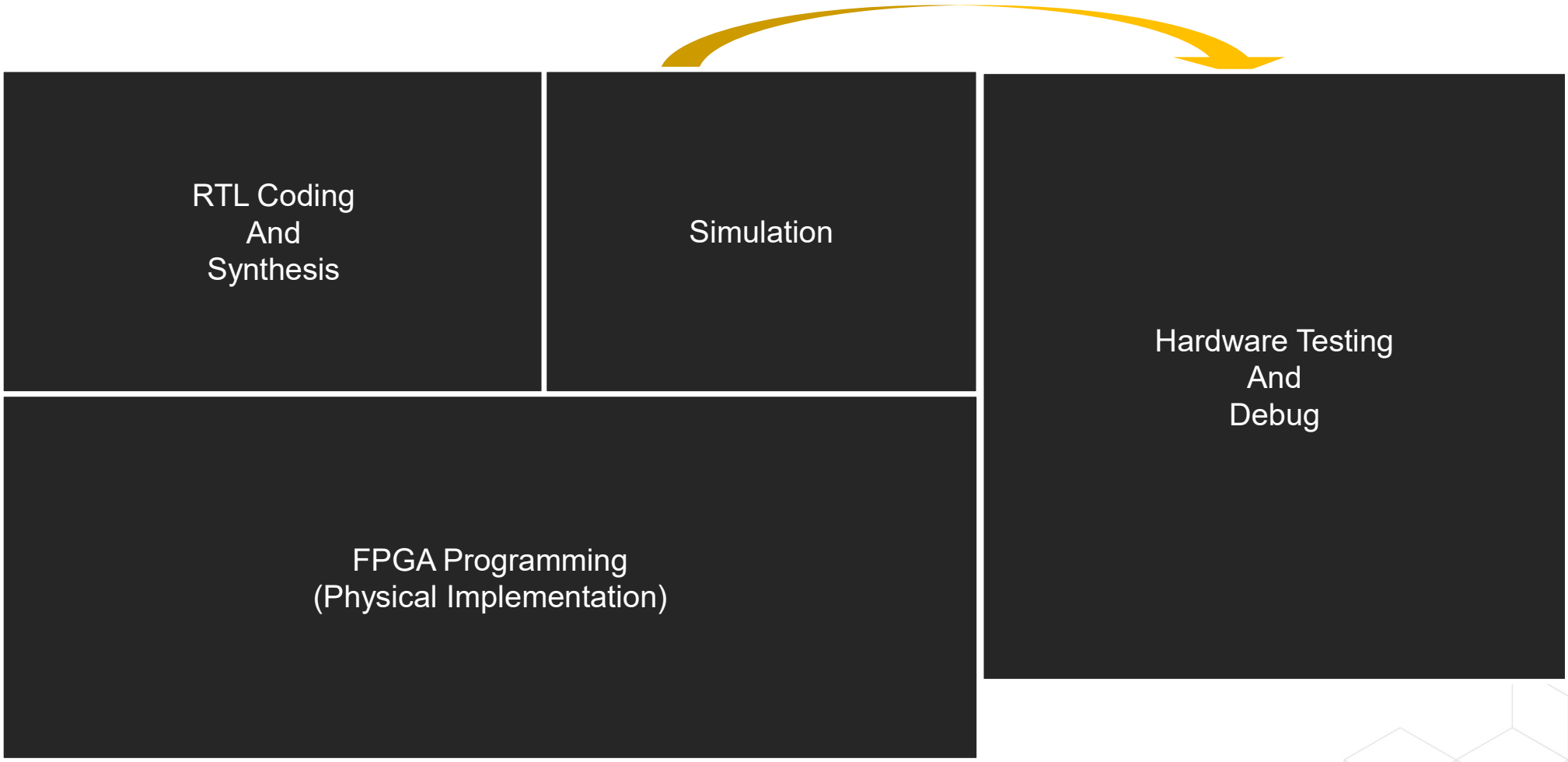
FPGA to ASIC: Gain Performance Potential to Remain Nimble

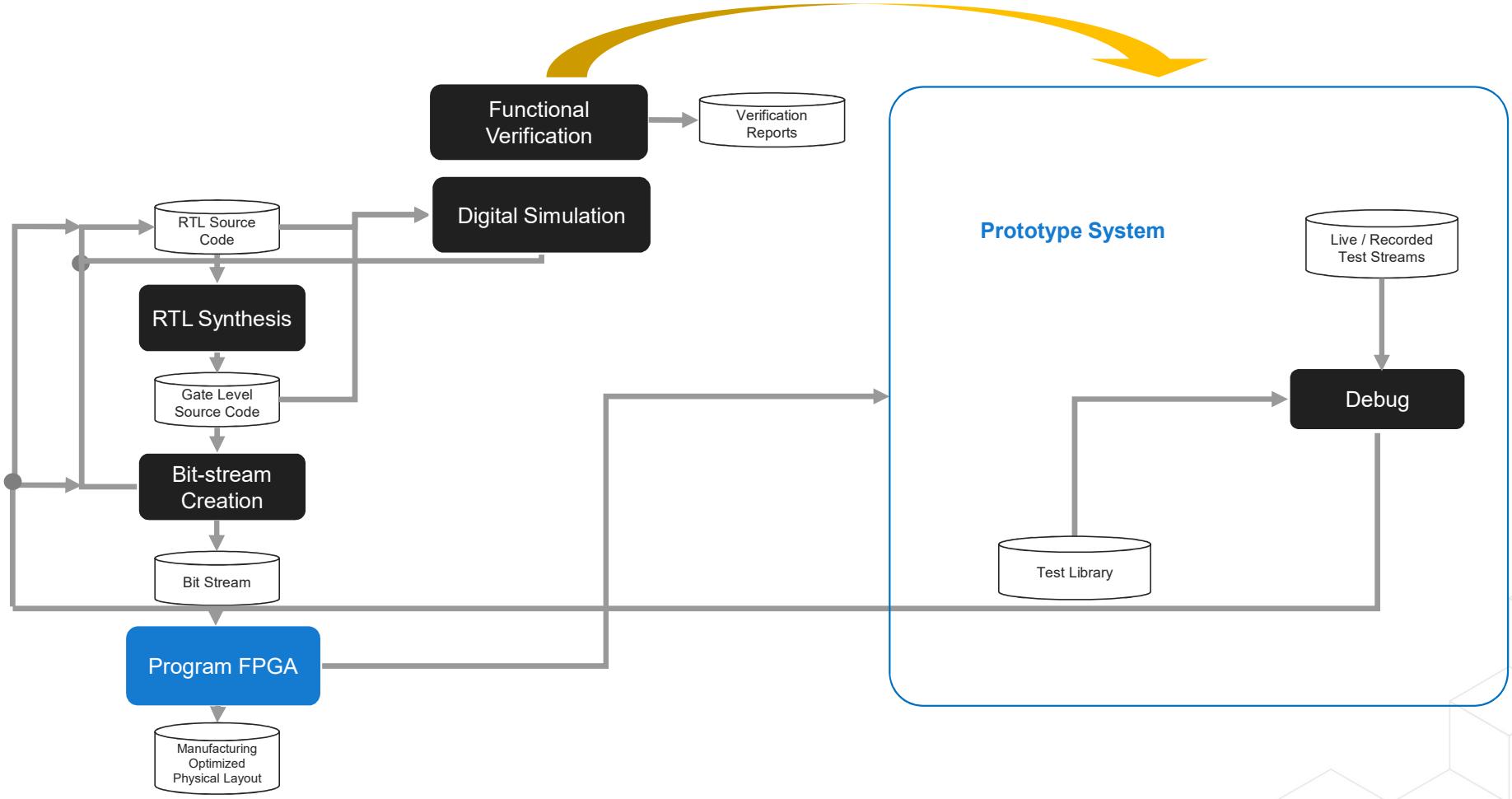
- ASIC removes system latency
  - Faster RX/TX ethernet
  - Faster memory subsystem
- Opens performance tuning options
  - Push more analytics to edge computing
  - Push more data to server analytics
- ASIC can also be nimble
  - Custom processor – SW programmable with unique instructions for low-latency
  - eFPGA – potential for reconfigurable logic



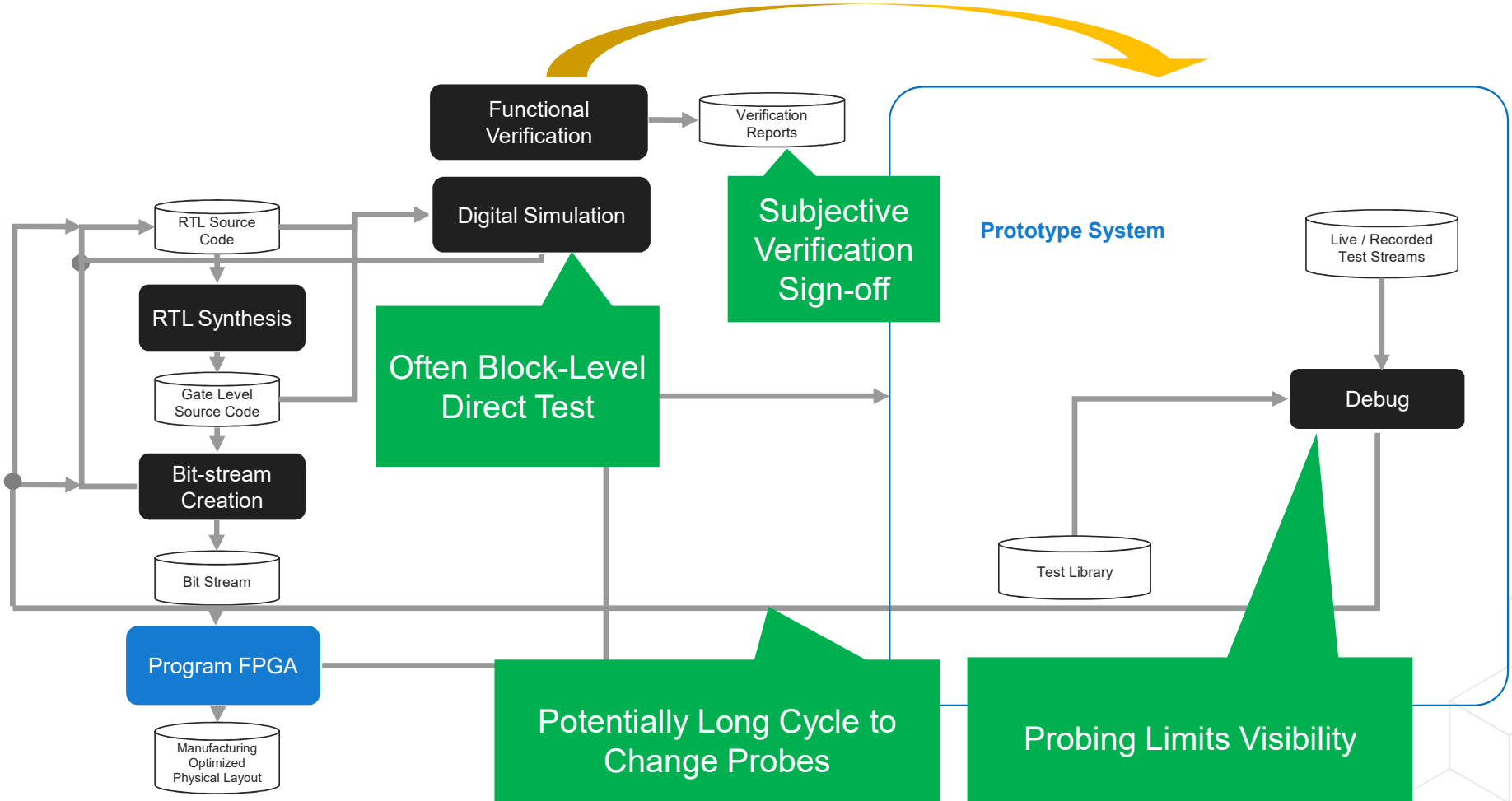
High-Level FPGA Development Flow



Detailed FPGA Development Flow

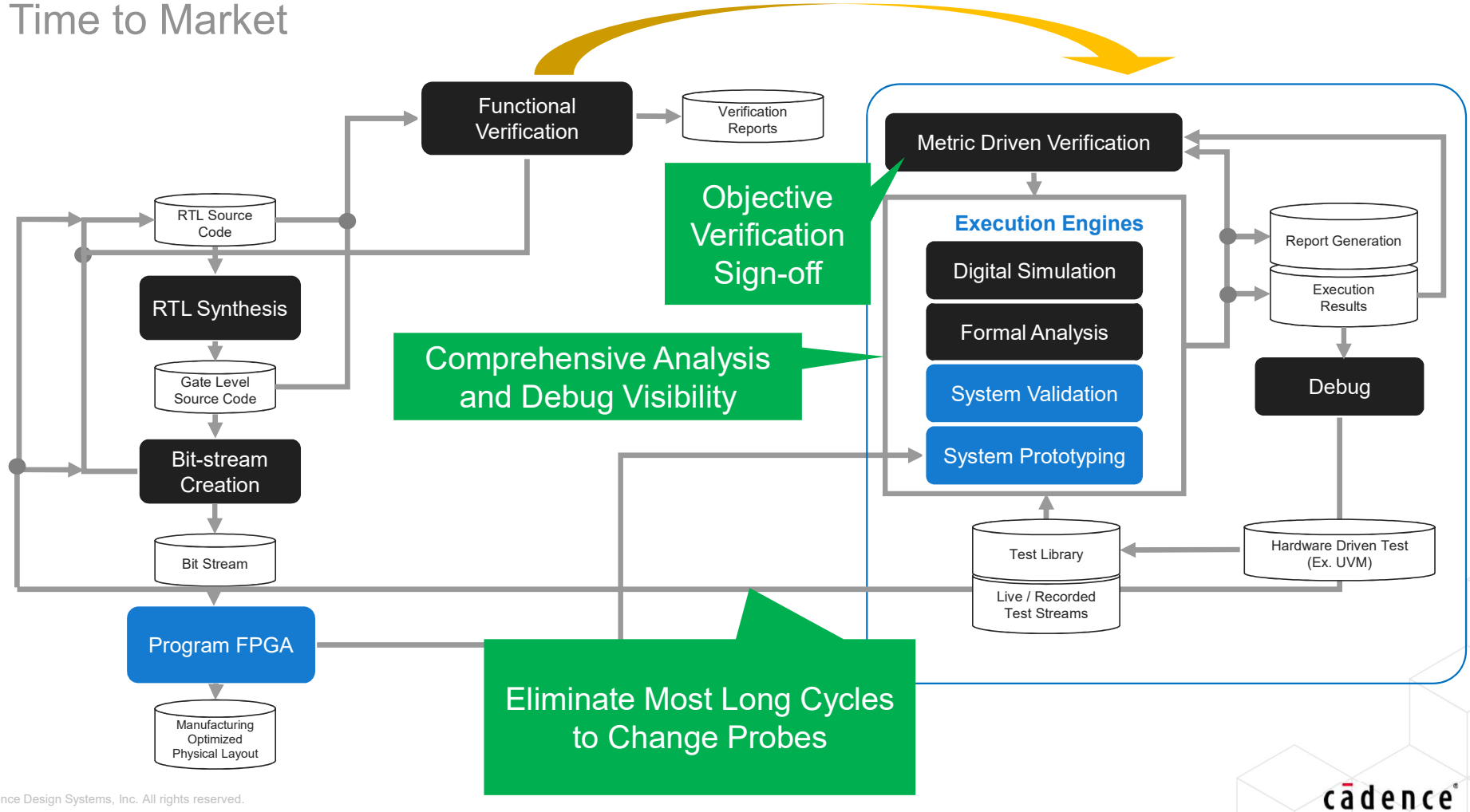


Detailed FPGA Development Flow With Verification Challenges

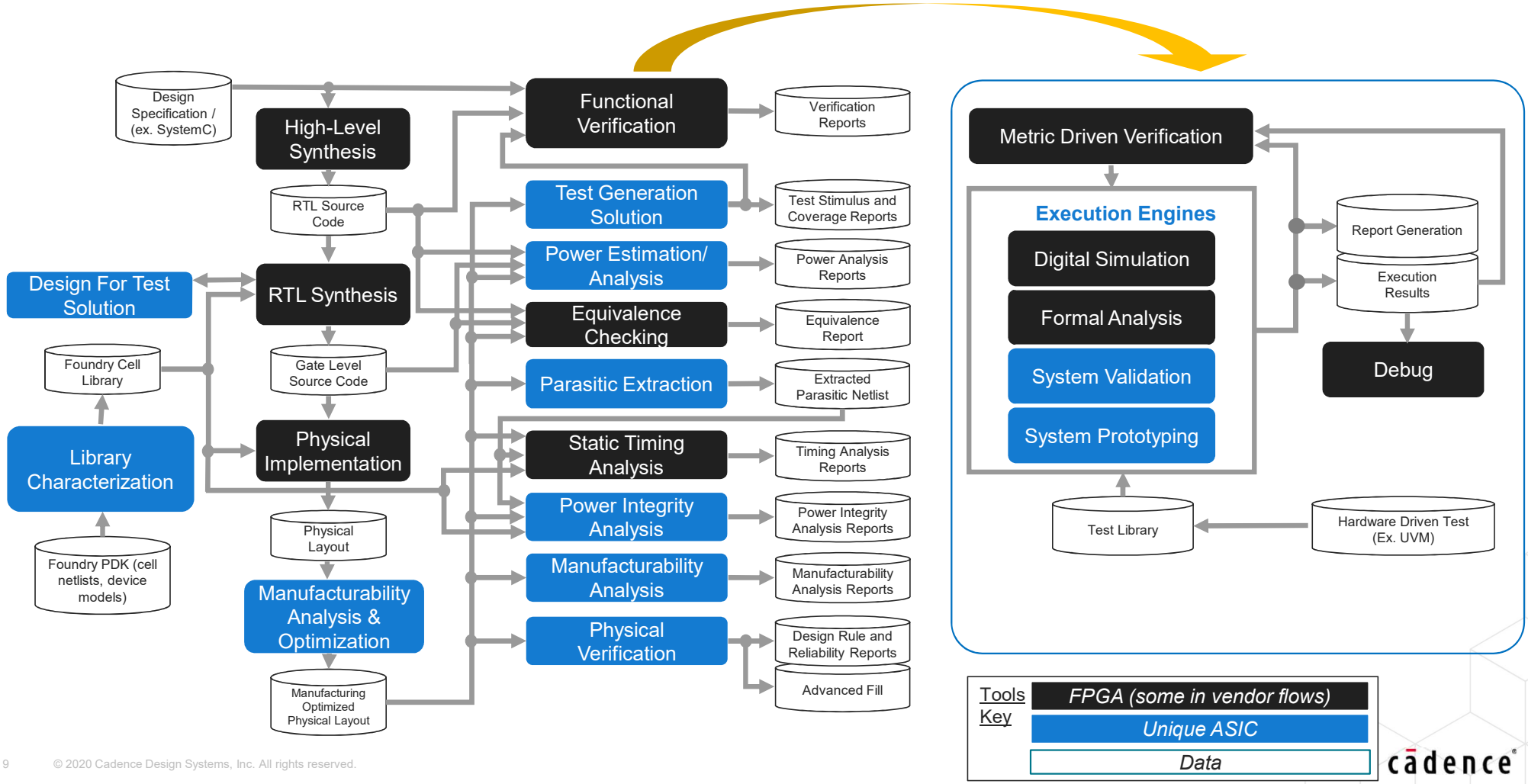


Detailed FPGA Development Flow With Quantitative Analysis

Faster Time to Market

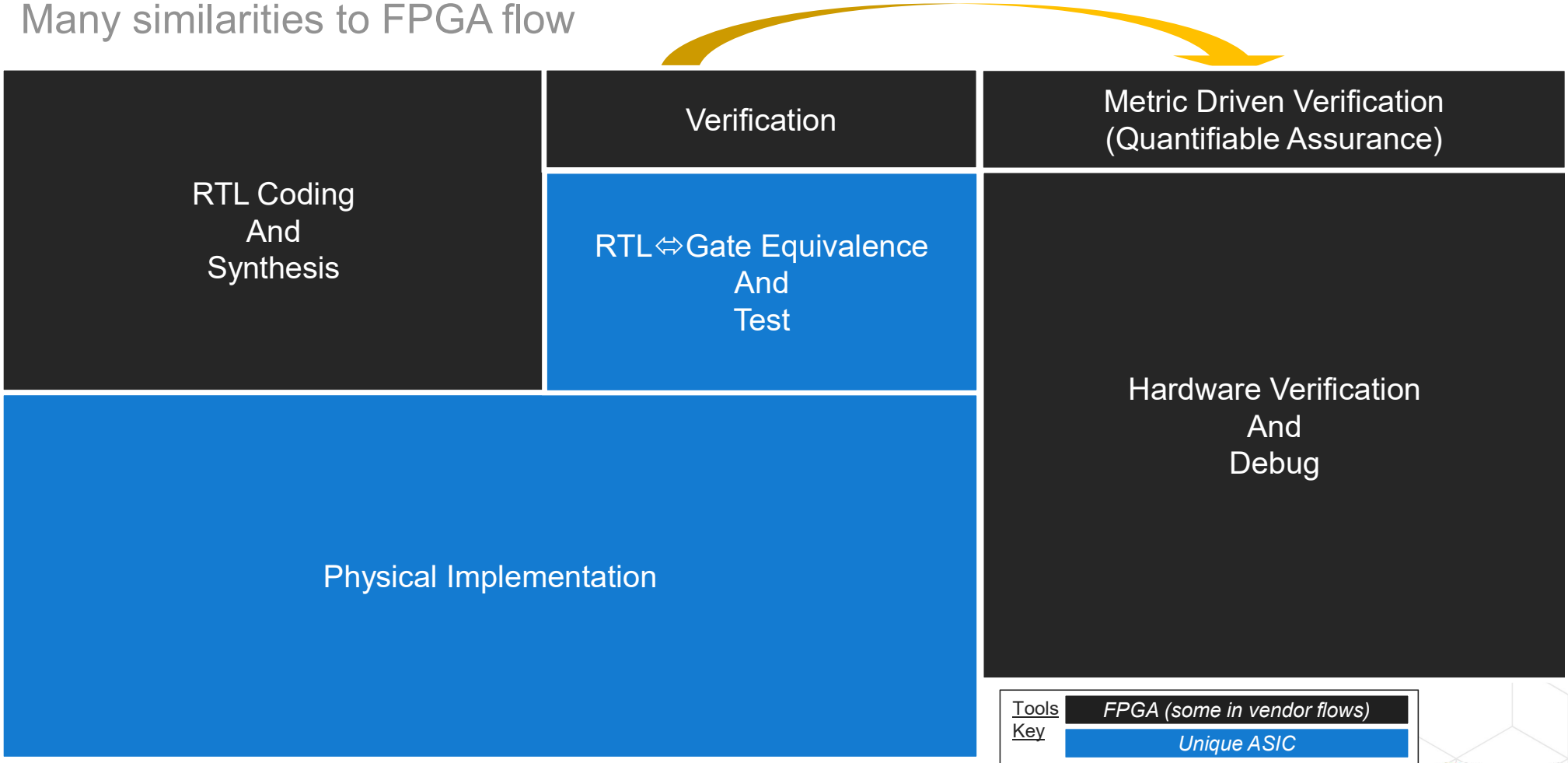


ASIC Flow Adds Foundry Methodology and Tools

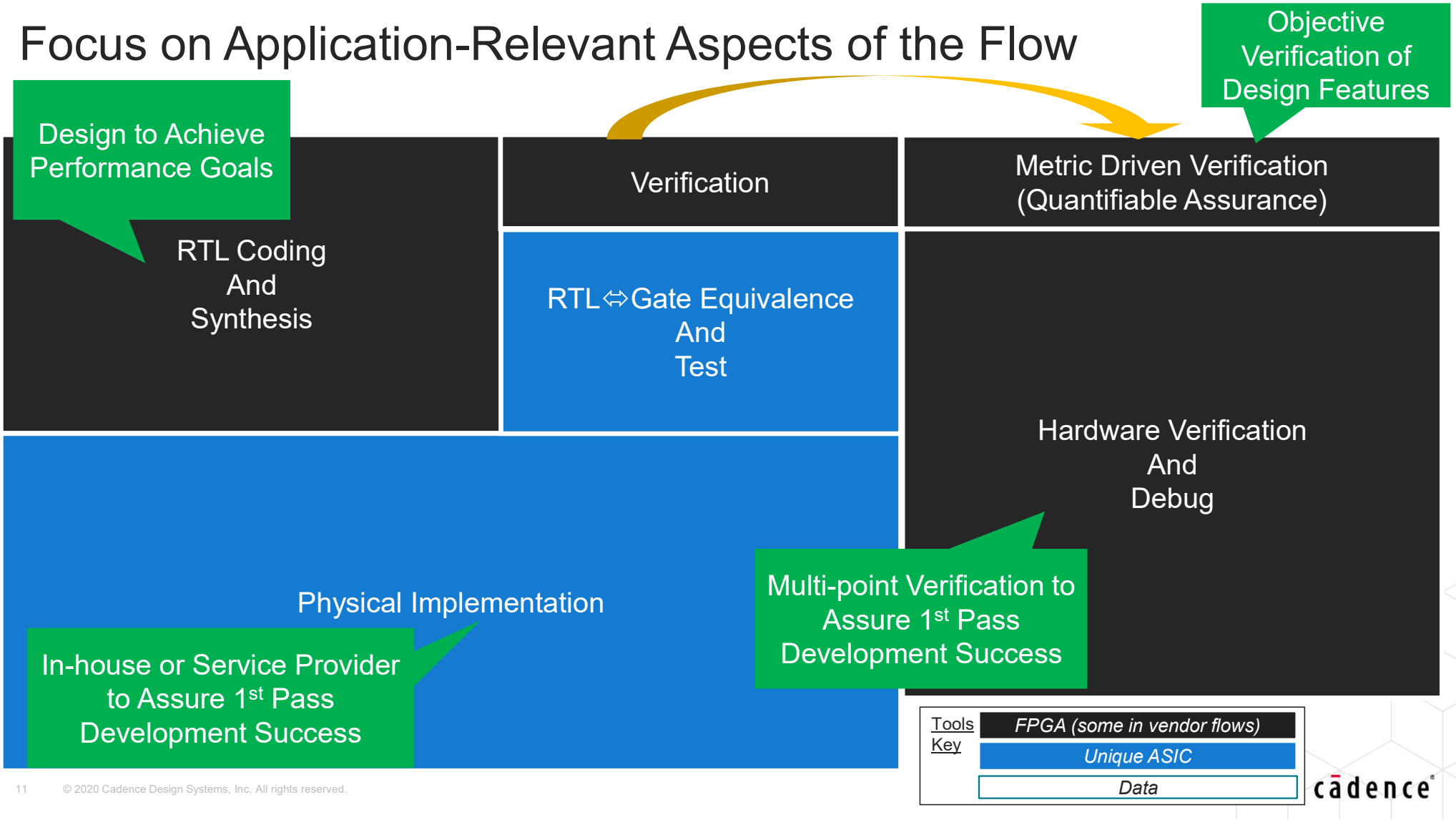


High-Level ASIC Flow Adds Foundry Methodology and Tools

Many similarities to FPGA flow



Focus on Application-Relevant Aspects of the Flow



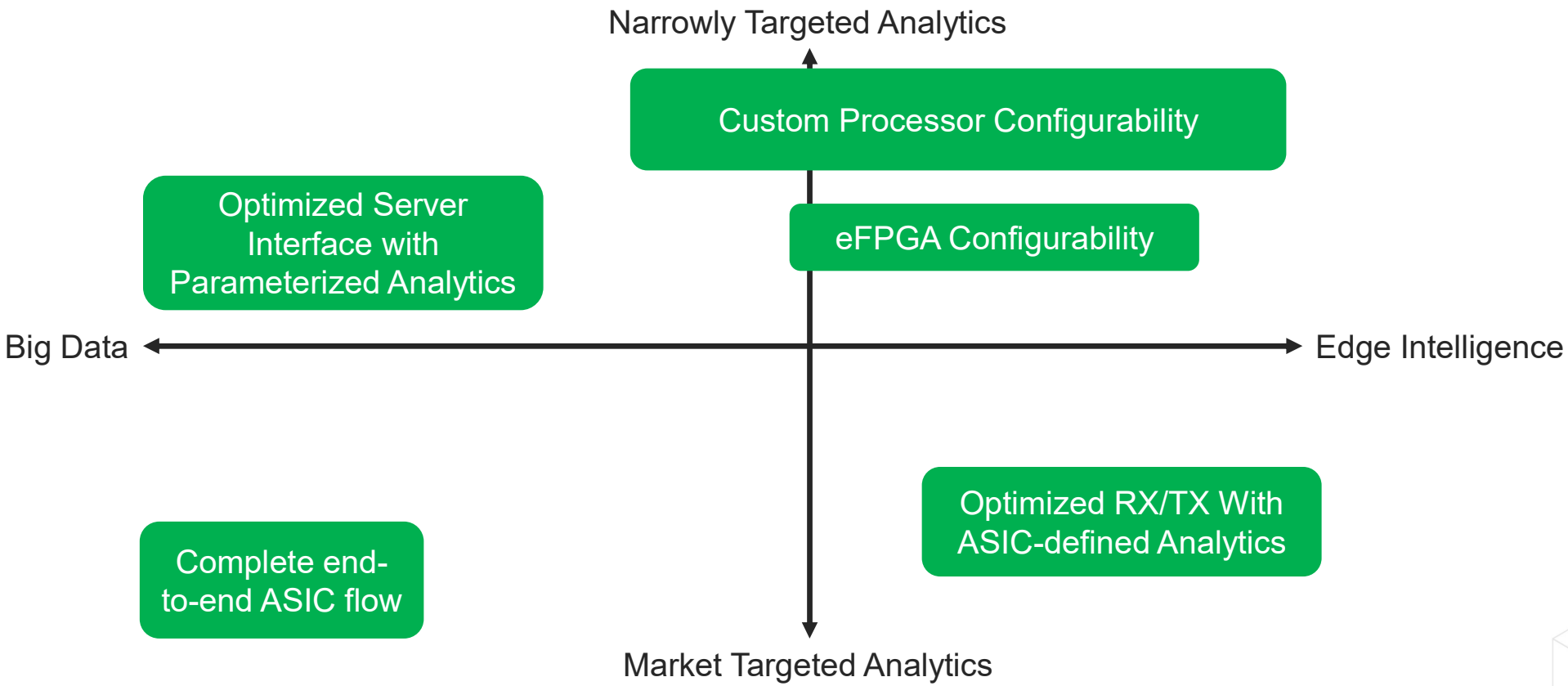
Adapting FPGA Development for ASIC

Flow Step	Adaptation	Engineering Skills	Decision Processes
IP	New IP source(s) aligned to foundry and process node	Hire/consult with process knowledge	• Identify critical IP used in FPGA flow • Evaluate custom processor to enable ASIC to be updated after production • Research foundry and process node • EDA provider and/or implementation service provider may have IP or be able to recommend
Digital Design	New synthesis and implementation tools	New training for synthesis, hiring for implementation	• RTL synthesis use similar to FPGA with new tools aligned to foundry and process node • Determine if in-house implementation flow provides application-relevant differentiation; otherwise outsource
Verification	More exhaustive tool suite	New training and refocus from prototyping to tools; may grow team	• **Start now! Faster time-to-market for FPGA with objective analysis of quality** • Shift toward verification automation is relevant for FPGA and ASIC due to growing complexity • Verification skills differ from digital design such that additional training may not be sufficient • Higher quality expectation may need additional resources

ASIC Concerns and Mitigation

ASICs are Fixed	• Focus fixed logic on communication architecture • Proven configurable processor enables SW flexibility • Emerging eFPGA can maintain HW flexibility
Time to Market is High	• Proven processes can execute in months • Updateable IP maintains reactive retargeting • Rigorous process tends to achieve better quality
Building Team is a Barrier	• Retraining and engineering resources available worldwide • Staged hiring leveraging design and verification services
High Development Cost	• ROI from lower latency offsets development cost • MPW runs in low (< 100) unit volume reduce foundry costs • Rigorous process offsets manual FPGA development costs

Implementation Path Defined By Financial Product Value Prop



Cadence is Your ASIC Partner

- Verification solution: apply objective analysis to improve FPGA and prepare for ASIC
  - Link to Tech Brief
- ASIC solution: broadly adopted in high-speed comms and mission-critical applications
- Tensilica IP: proven processor technology used in autonomous drive and other high-reliability apps
- High-perf IP: proven in leading comms systems
- Services: expert RTL to GDS design services