



**The New  
Global Standard in  
Ultra-Low Latency &  
Ultra-High Capacity Messaging**

**Zero Impact Message Validation in a Hardware Device**



# Mutually Exclusive

## Safety Conflicts With Performance

- **Network Transmissions Subject to Security/Regulatory/Counterparty Validation Processing**
- **Validation Processing Creates Introduced Latency**
- **Introduced Latency Negatively Impacts Latency-Sensitive & Latency-Intolerant Transmissions**
- **Business Dictates Drive Minimization of Validation Processing and Acceptance of Increased Risk**
- **Acceptance of Increased Risk Underpinned by “It Can’t Happen to Me” Beliefs**

*It Can't Happen to Me?*



# Progress But No Solution – Until LMS...

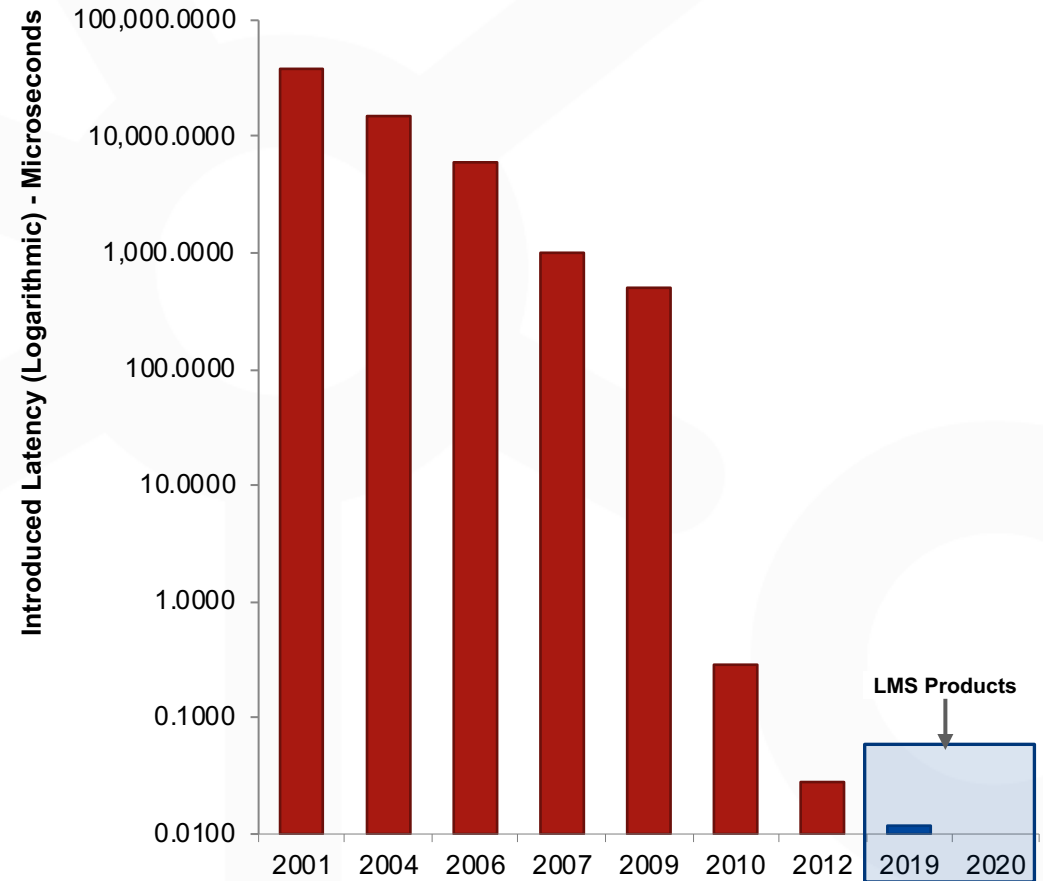
Introduced Latency Reduced But Not Eliminated

- **Legacy FIX Systems Replaced by Native-Protocol Software and Hardware Solutions; Latency Reduced to Single-Digit Microseconds**
- **Native-Protocol Solutions Evolved from Layer-4 to Layer-2; Latency Reduced to Hundreds of Nanoseconds**
- **Introduction of New Regulations Mandating Specific Requirements and Methodologies Exacerbated Tensions**

**While...**

- **15+ Years of Commission Compression Have Crushed Broker Economics Reducing Investment, Innovation & Choice**

**Evolution of Introduced Latency**

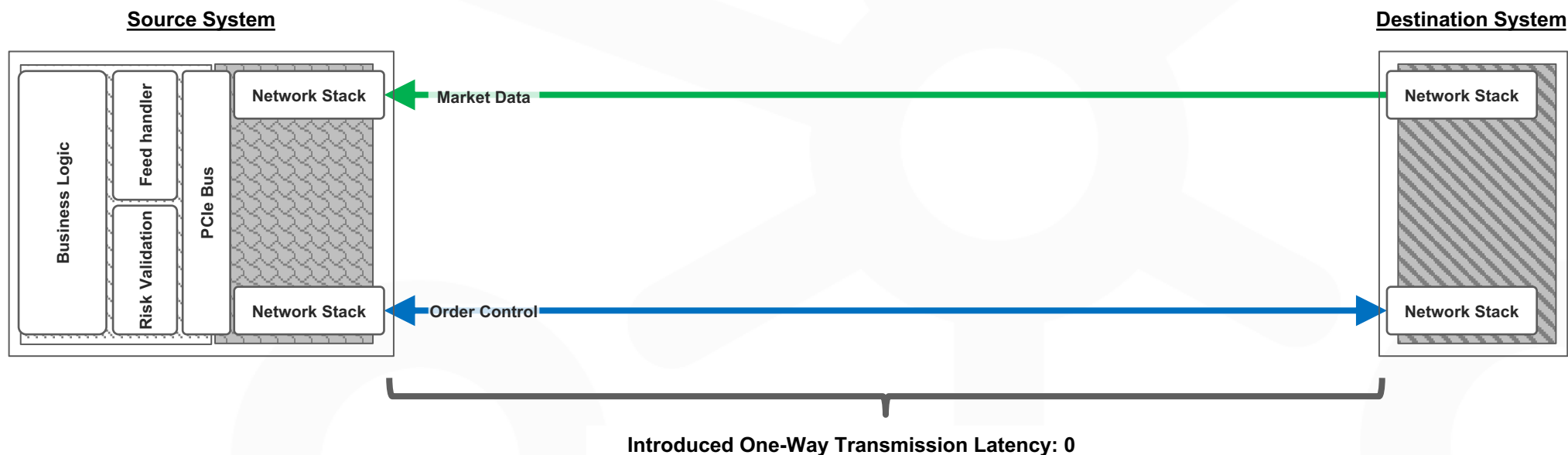


*Safety Has Conflicted With Performance, Until Now...*



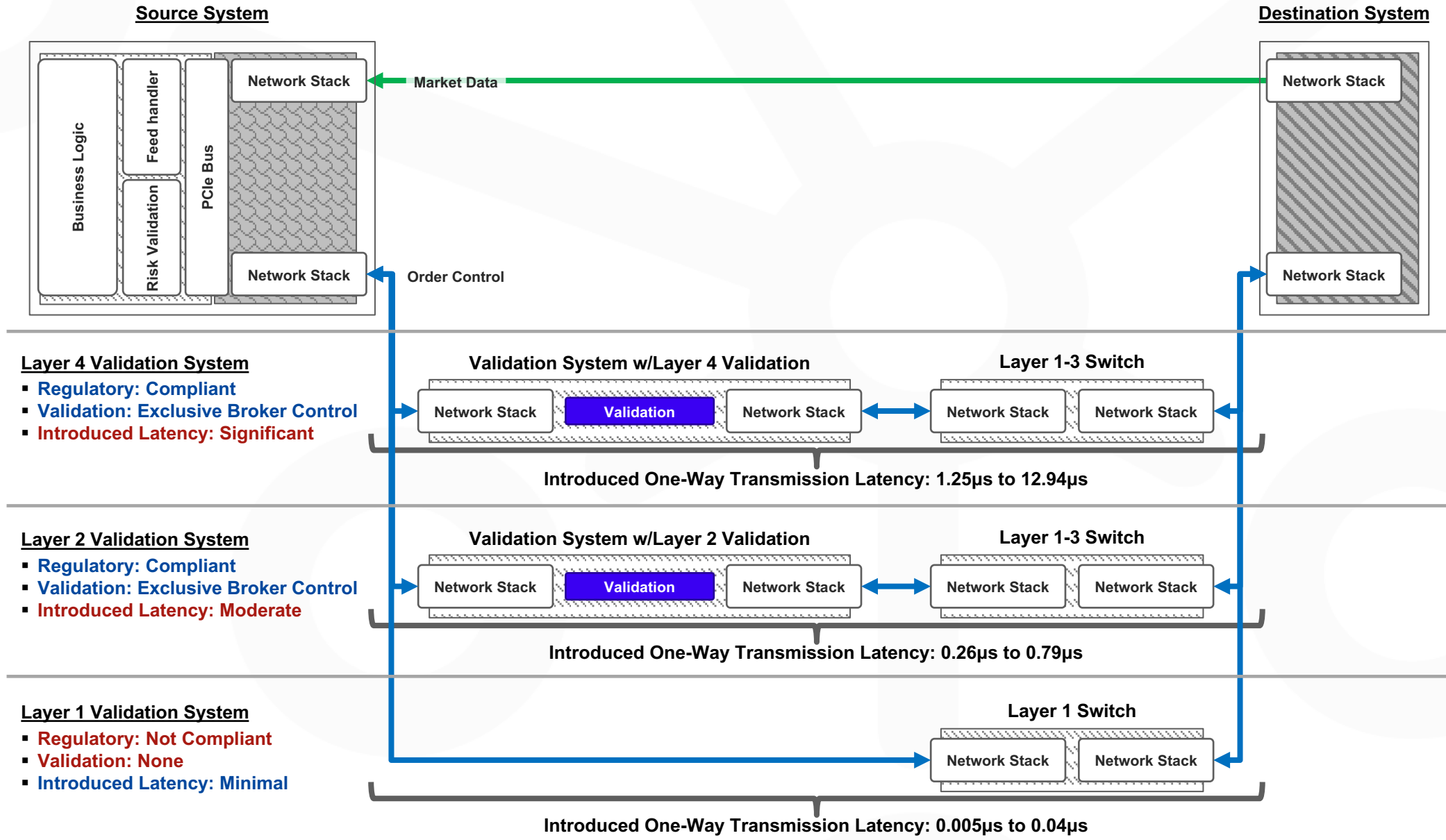
# Ideal Outcome

Latency Intolerant Transmissions Demand a Direct Connection



# Current Reality

Existing Solutions Deliver Constraints, Forced Compromises, or Non-Compliance and Risk

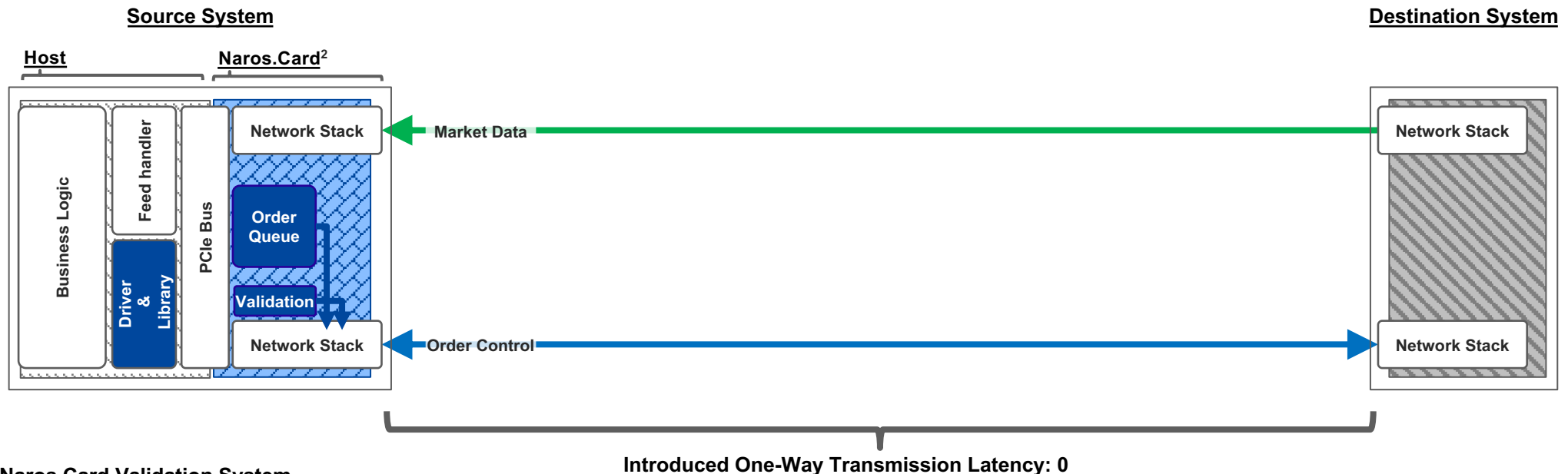


# Naros.Card: Zero Impact. Zero Introduced Latency. End-to-End.

Direct Connection Market Access w/Zero Impact Message Validation

## Key Outcomes

- **Signal-To-Trade: 118.54ns<sup>1</sup>**
- **Full Stack: Rx: 234.08ns<sup>1</sup> (205byte payload); Tx: 28.21ns<sup>1</sup>**
- **Rx to PCIe to Software to PCIe to Tx: 1.1µs (First Bit In to First Bit Out, Full Rx of 18 Byte Packet)<sup>1</sup>**



## Naros.Card Validation System

- **Regulatory: Compliant**
- **Validation: Exclusive Broker Control**
- **Introduced Latency: Zero**

<sup>1</sup>Not a STAC Benchmark; STAC Benchmark Testing Schedule TBD; <sup>2</sup>US Patents 9,501,795 & 10,269,071; Others Pending

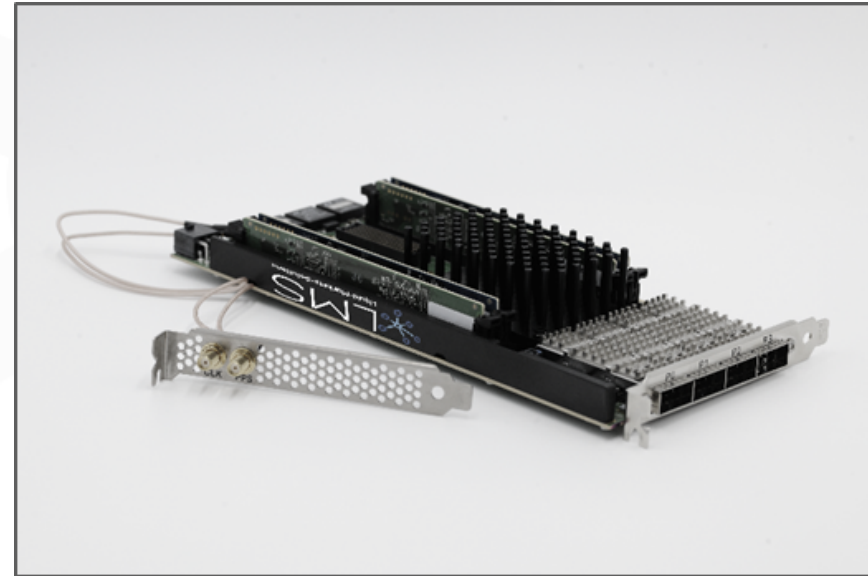


# Naros.Card - Science not Magic

Direct Connection Market Access w/Zero Impact Risk Mitigation

## Key Points

- Delivers Zero Introduced Latency
  - Complete Parallelization
  - Direct Market Connectivity
- Ultra-Performant TCP/IP Stack
- Ultra-Performant Kernel Bypass
- Multi-Dimension Message Queuing
- Market Native or Binary Protocol
- Comprehensive Risk Mitigation
- Exclusive Control via Encrypted Logic



US Patents 9,501,795 & 10,269,071; Others Pending

*The Solution for the Most Performance-Demanding Latency-Intolerant Trading Strategies*





A black and white photograph of Lewis Hamilton in the cockpit of a Mercedes Formula 1 car. He is wearing a racing helmet with the Mercedes logo and 'PETRONAS' and 'EPSON' branding. The car's bodywork features various sponsor logos including 'PETRONAS', 'EPSON', and 'Mercedes-AMG Petronas Formula One Team'.

## Safety and Performance

Zero-Impact Regulatory/Counterparty/Security Validation

## Effective and Effortless Control

Market, Counter-Party, and Cyber-Security Message Validation

- **Advanced Cyber-Security**
  - Application-Specific Firewall
- **Powerful and Flexible**
  - Security-Specific Lookup
  - Firm/Desk/Trader-Specific Lookup
- **Fast Adoption**
  - Comprehensive Methodology
  - Entity-Exclusive Control
- **Regulatory-Compliant**
  - Pre-Trade Validation
  - Post-Trade Surveillance

*Multi-Scope Approach Optimizes Risk Mitigation*

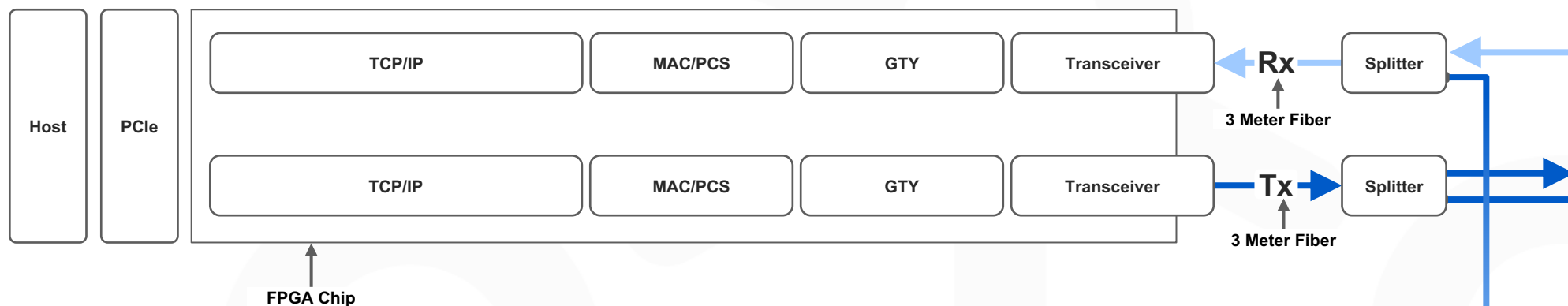


# Appendix 1: Latency Measurement Methodology

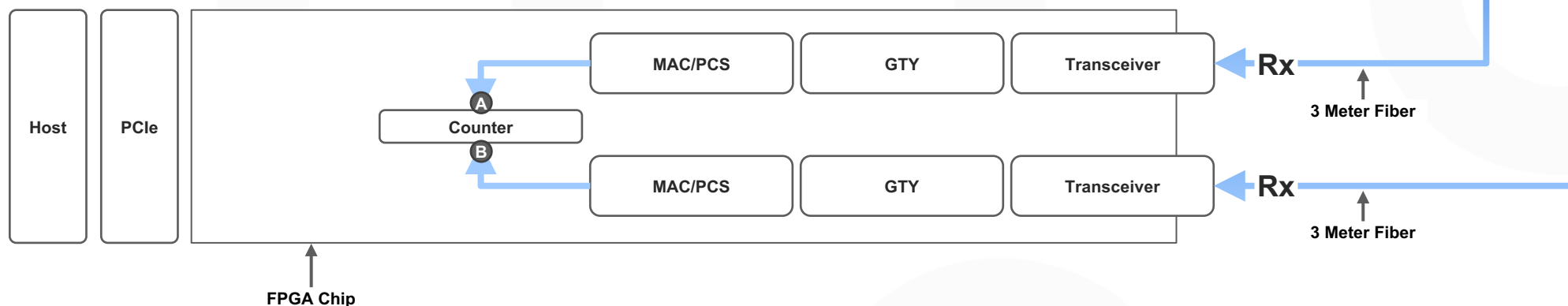
## Validation of Internal Measurements via External Observation

- Inbound and Outbound Fiber Signals Split, Transmission Received by Detector
- 1<sup>st</sup> bit of Inbound Frame Triggers Counter Start; Point “A”
- 1<sup>st</sup> bit of Outbound Frame Triggers Counter Stop; Point “B”
- Latency:  $((\text{“B”} - \text{“A”}) * \text{Clock Frequency}) - 6 \text{ Meter Fiber Latency}$

### Test Object

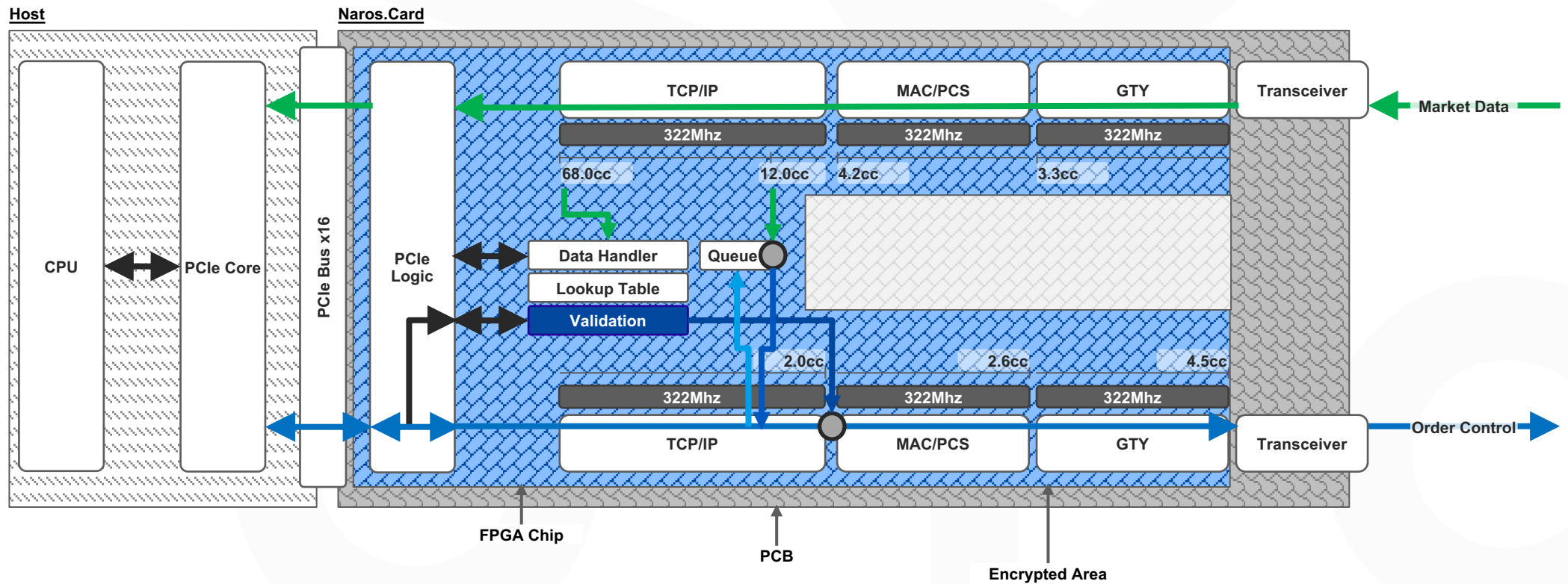


### Detector



# Appendix 2: Naros.Card<sup>1</sup> 10GbE Function Performance

## Function Schematic and Latency Summary



<sup>1</sup>US Patents 9,501,795 & 10,269,071; Others Pending

# Naros.Card Redefines Reality

Direct Connection Market Access w/Zero Impact Message Validation

**ZERO IMPACT. ZERO INTRODUCED LATENCY. END-TO-END.**

**FULLY REGULATORY COMPLIANT. GLOBALLY.**

**UNIQUE YET PROVEN. LEVERAGES PATENTED & PATENT-PENDING TECHNOLOGY.**





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