STAC Fast Data Update

Peter Nabicht
Head of Strategy, STAC

peter.nabicht@STACresearch.com

STAC Fast Data Update

- FPGA Special Interest Group (SIG)
- Pre-trade risk benchmarking

STAC®
SECURITIES TECHNOLOGY ANALYSIS CENTER

FPGA SIG: context

- FPGA usage continues to grow in a variety of areas in finance
  - Accelerated network I/O
  - Market data processing
  - Execution of realtime trading logic
  - Pre-trade risk computation
- Previous discussions of FPGA use have been focused on the *why* use FPGA and *what* use cases are best fits for FPGA
- But discussions are rarely about *how* to implement and manage custom FPGA solutions

FPGA SIG: background

- Panel from Global STAC Live spring 2020
  - Moving FPGA forward on the maturity curve
- Received feedback that this was the type of conversation around FPGA that the industry needed more of
- People were actively seeking interaction
  - A way to speak about needs with one voice
  - A forum for discussing non-proprietary challenges and solutions in FPGA development

FPGA SIG: status

- STAC FPGA SIG been formed off the back of this initial interest
- First call was held on Oct. 7
- While the group's mission will evolve, initial objectives are:
  - Facilitate dialog regarding common challenges in FGPA design, development, testing and deployment
  - Articulate industry requirements for FPGA hardware and toolchains where commonalities exist
  - Outline a series of best practices in the development and use of FPGA in financial services

www.STACresearch.com/fpga

FPGA SIG: members

- Initially formed with the involvement of 7 financial firms, including:
  - Exchanges
  - Dealers
  - Proprietary trading firms
  - Hedge funds
- Looking for more financial firms to increase the collective voice of group
- Want to establish a direction and framework for interaction and then planning on working with vendors, including:
  - Hardware providers
  - Tooling providers
  - Functionality providers

FPGA SIG: next steps

- The first call established some concrete next steps
  - Create a discussion forum for FPGA development, testing, and deployment (now live at STACresearch.com/fpga)
  - Work together to create a wish list for discussion with FGPA hardware vendors
  - Another call to further discussion on the wish list and discuss similar regarding tooling
- The next call will happen in mid-November
  - If you'd like to join the call it is not too late to participate

www.STACresearch.com/fpga

FPGA SIG: discussion, not benchmarks

- Not intended as group for the creation of FPGA benchmarks
- The most commonly applied benchmarks to FPGA (so far):
  - STAC Network I/O SIG (https://www.stacresearch.com/nio)
  - STAC-TS (https://www.stacresearch.com/ts)
- And maybe more benchmarks applied in the future
  - There are STAC-A2 on FPGA results in the STAC vault already
  - Already talk of FPGA for other analytic workloads, such as backtesting, ML training, and ML inference

Pre-trade risk benchmarks

- STAC has received renewed industry interest around pre-trade risk benchmarks
- Multiple solutions in the markets without like-to-like comparisons of:
  - Latency impact
  - Throughput
  - Functionality
- Vendors and financial firms want to compare different external options as well as current in-house solutions

Pre-trade risk benchmarks: status

- Have begun discussing the framework and scope of pre-trade risk benchmarks with a couple of firms
- Benchmarks for pre-trade risk would need to:
  - Quantify the throughput / capacity of the stack under test (SUT)
  - Measure the latency at different loads
  - Measure the latency of different risk check functionalities
  - Verify that the functionality works as expected
- Looking to take these initial interests to the next step

Pre-trade risk benchmarks: call for interest

- Want more voices in the discussion
- If there is sufficient interest, we'll form a working group
- If you are interested in participating, please contact me

peter.nabicht@STACresearch.com