

ARISTA

daves@arista.com

Copyright © Arista 2022. All rights reserved.

SwitchApp - Now the fastest* Layer 3 switch too

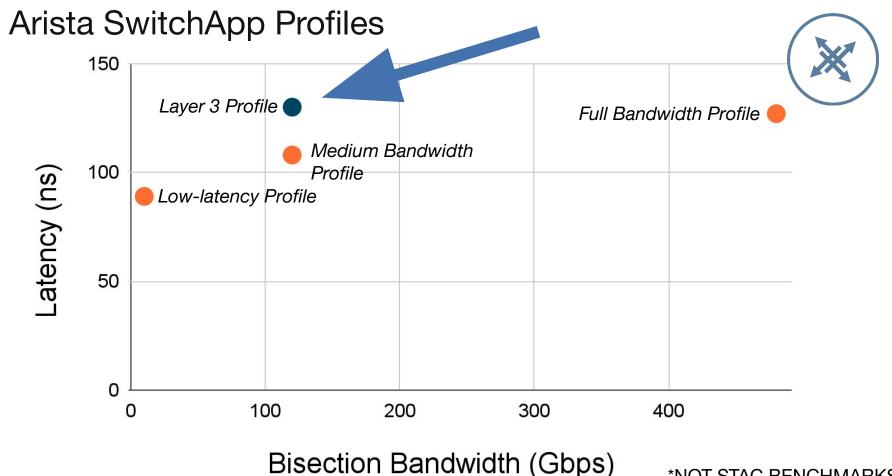
X

- Full-featured 1/10G Layer 2/3 switch -- implemented in FPGA
 - Ultra-low latency packet forwarding averaging 89 ns (L2) or 133 ns (L3)
 - Full cut-through architecture
 - 48x 1/10G ports
 - 10k Uni- or multicast MAC addresses
 - 30k unicast, 22k multicast routes
- Fully integrated with EOS, running on 7130LB devices
 - Standard EOS CLI and protocols: STP, LLDP, IGMP, LAG
 - Standard EOS L3 stack: BGP, PIM, OSPF
 - Standard Management, telemetry, protocols, forwarding plane, CloudVision
- Layer 3 features are now generally available from EOS 4.28.0F
 - Download at: https://mako.arista.com/dyn/softwareportal/releases/#switchapp

SwitchApp looks, feels and tastes like any EOS switch

*NOT STAC BENCHMARKS

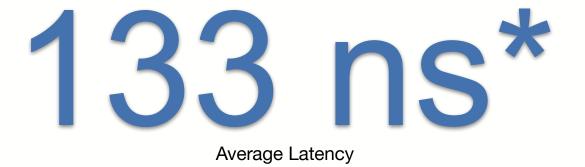




*NOT STAC BENCHMARKS

SwitchApp - Now the fastest* Layer 3 switch too





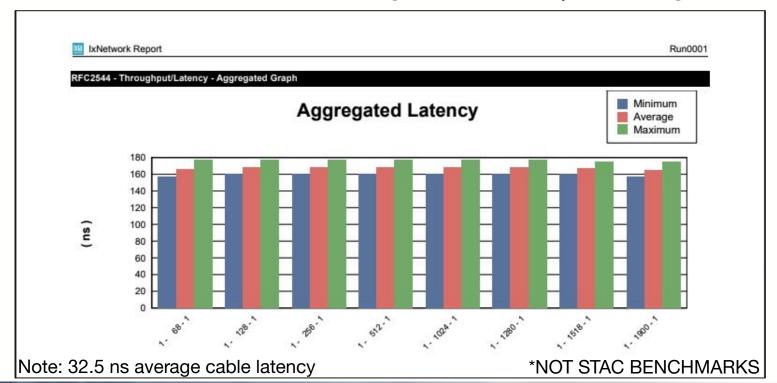
SwitchApp looks, feels and tastes like any EOS switch

*NOT STAC BENCHMARKS



Full cut-through

RFC2544 tests show full cut-through for all tested packet lengths



Introducing 7130LBR and 7130B



7130LBR with

Broadcom Jericho 2

48x SFPs and 6x QSFP-DD (NRZ)

- Converged Layer 1 and L2/3 switch
- FPGAs for market edge applications



7130B with

Intel Tofino

32x QSFP-DD (NRZ)

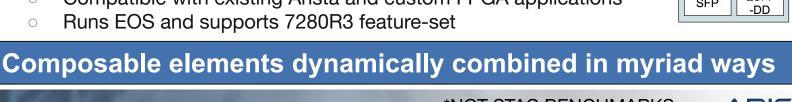
- 256-lane converged L1/2/3 switch
- Scaling out Layer 1 networks

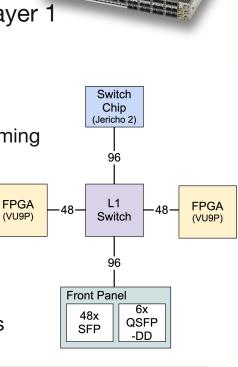
Converging Layer 1 with Layer 2 / 3 for scale



Introducing 7130LBR-48S6QD

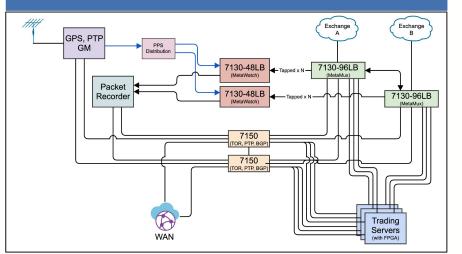
- Agility: Key composable elements, fully connected via Layer 1
 - External connectivity 96 front panel ports
 - Full-featured Broadcom Jericho2 switch 96 interfaces
 - FPGA applications Two 48-port programmable FPGAs
 - High precision timing Integrated GPS and Atomic Clock
 - Performant 6* ns Layer 1, 40* ns muxing, 16* ps resolution timing
- Innovation: Fully integrated device
 - >2.5x Capacity in less than 1/3rd the space
 - High density QSFP-DD significantly reduces cable count
 - All-in-one solution eliminates inter-device latency
- Simplified: Trade network to exchange edge
 - Compatible with existing Arista and custom FPGA applications
 - Runs EOS and supports 7280R3 feature-set



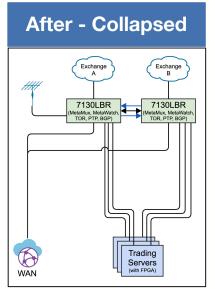


7130LBR Use Case: Converged Trade edge

Before - Multiple devices and tiers



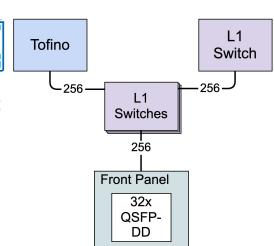




Typical Small Deployment	Existing Trading Infrastructure	7130LBR Composable Trading Infrastructure	Impact
Number of devices	8+ devices, 11 RU footprint	2 devices, 2 RU footprint	75%+ Reduction in devices, rack space
Number of cables (excl. servers)	Over 100 interconnections	<10 interconnections	75%+ Reduction in cabling
Typical Power Consumption (W)	2200 W	800 W	65% Reduction in power consumption

Introducing 7130B-32QD

- Agility: Highest density, fully connected via Layer 1/2/3
 - External connectivity 256 front panel ports
 - Full-featured Intel Tofino switch 256 interfaces
 - Ultra-low latency 7* ns port-to-port
- Innovation: Fully integrated device
 - >2.5x Capacity in less than 1/10th the space
 - High density QSFP-DD significantly reduces cable count
 - Integrated P4 Programmable switch chip
 - Scale-out solution eliminates inter-device latency
- Simplified: Trade network to exchange edge
 - Compatible with existing Arista profiles
 - Runs EOS and supports 7170 feature-set and custom P4



Composable elements dynamically combined in myriad ways

Bringing it all together – A fabric for composition

Use case: Connect **FPGAs** to **services**

- 7130B as a dense spine
 - Connected via QSFP-DD
 - L2/3 switching
- 7130LBR as a leaf
 - Connect to many markets
 - Timestamping, aggregation
 - Replicate market data to spines

Allows low latency, arbitrary changes.

Observability + automation = safety

