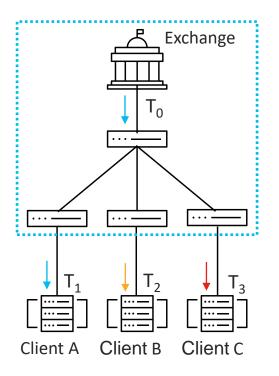


Fairness through a picosecond lens

Solution for Equitable Market Data Distribution

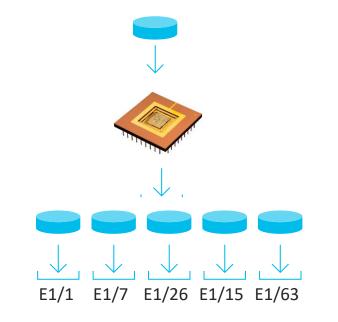
John Sabasteanski Distinguished Engineer STAC Summit – June 1, 2022

Problem – Market Data Distribution

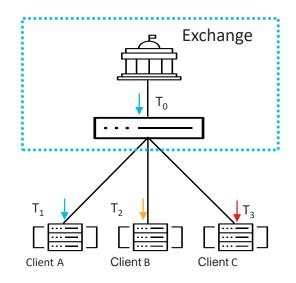


- Exchanges provide market data to various clients
- Exchange distributes data at time T₀
- Assumption is that each trader receives market data at same time, time T₁
- However, these clients often receive data at different times

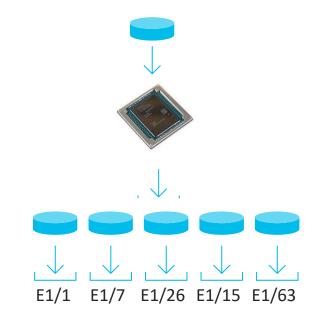
ASIC Based Multicast Replication



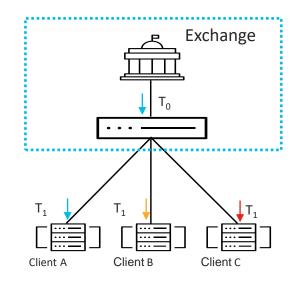
- ASIC multicast replication is serial
- Results in latency variation to egress ports (~21ns on N3K-C3548)



FPGA Based Multicast Replication



- FPGA multicast replication can be parallel
- Result is nearly simultaneous delivery



Nexus 3550-T FPGA Switch Delivers Unmatched Fairness

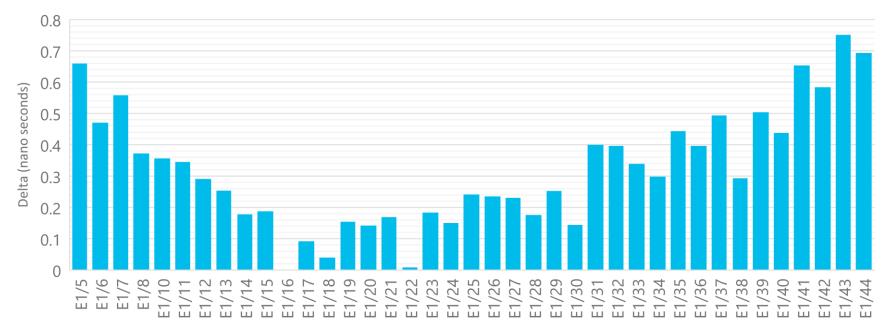


	Cisco	NX-OS support		Same NXOS CLI Same APIs Support in NDFC
	Low L	atency Layer 2 and	3	Port to port latency 100-160 nano seconds*, 25G capable
		FPGA		Xilinx Ultrascale+ VU35P-3 FPGA with 8GB HBM2
liates. All rights reserved.	Cisco Public	Custom FDK Design FPGA application on the switch		

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*Not STAC Benchmark

Nexus 3550-T Market Data Fairness*



Switch front Panel Ports

Per port delay from fastest port in this sample – all ports are inside of 1ns

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*Part of future NXOS software release Not STAC Benchmark

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The bridge to possible