



METAMA KO

Update from Metamako

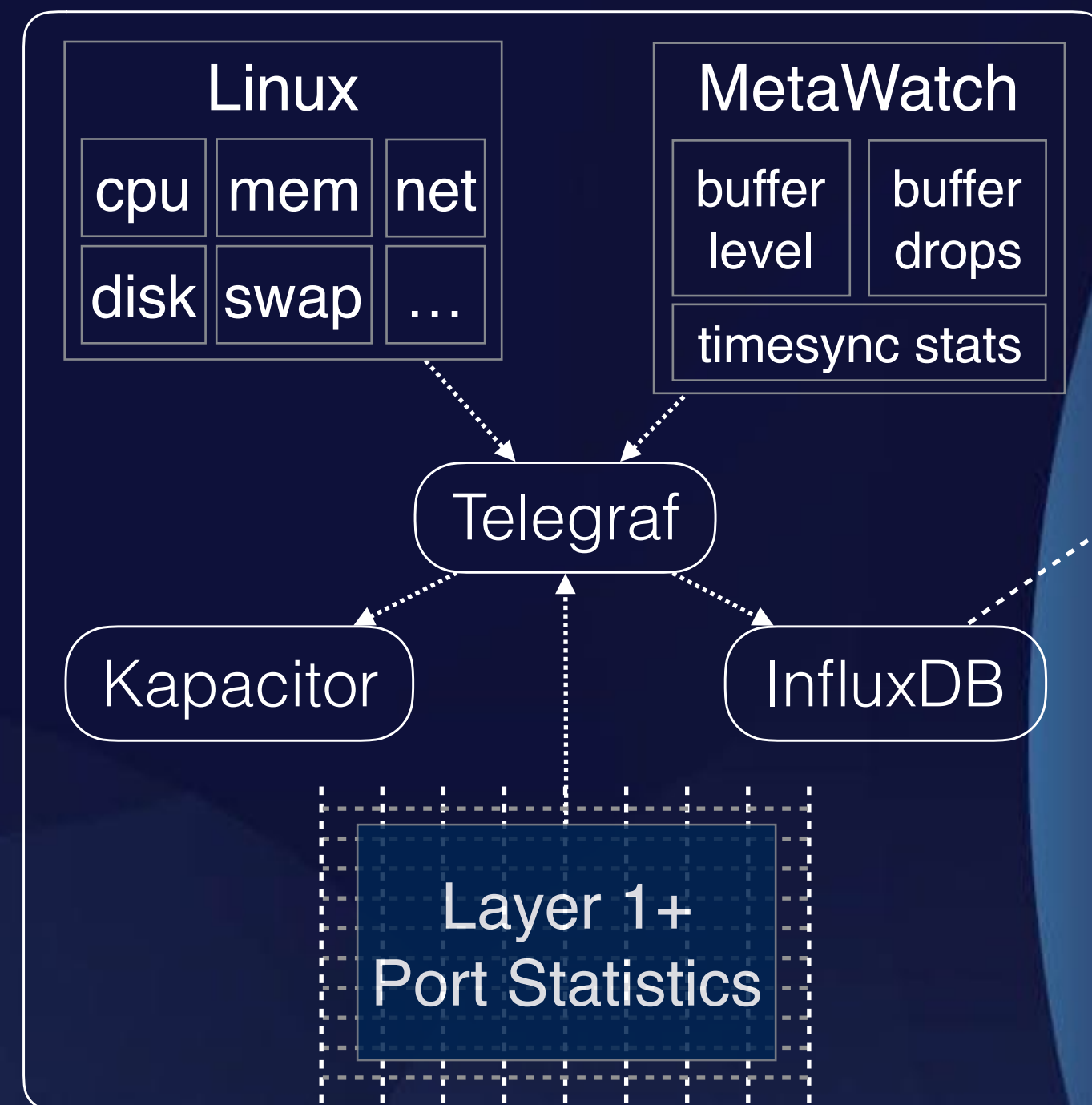
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VP of Technical Marketing
November 2017**

**Simplifying networks
Reducing latency in Electronic Trading
Opening up network packet visibility
Increasing flexibility**



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Telemetry: actionable real-time counters



Preconfigured on every device

- Real-time streaming counters from:
 - Linux
 - L1+ Port Counters
 - MetaWatch

Feeding local InfluxData Stack

- Telegraf - collection agent
- InfluxDB - time-series database
- Kapacitor - alerting engine

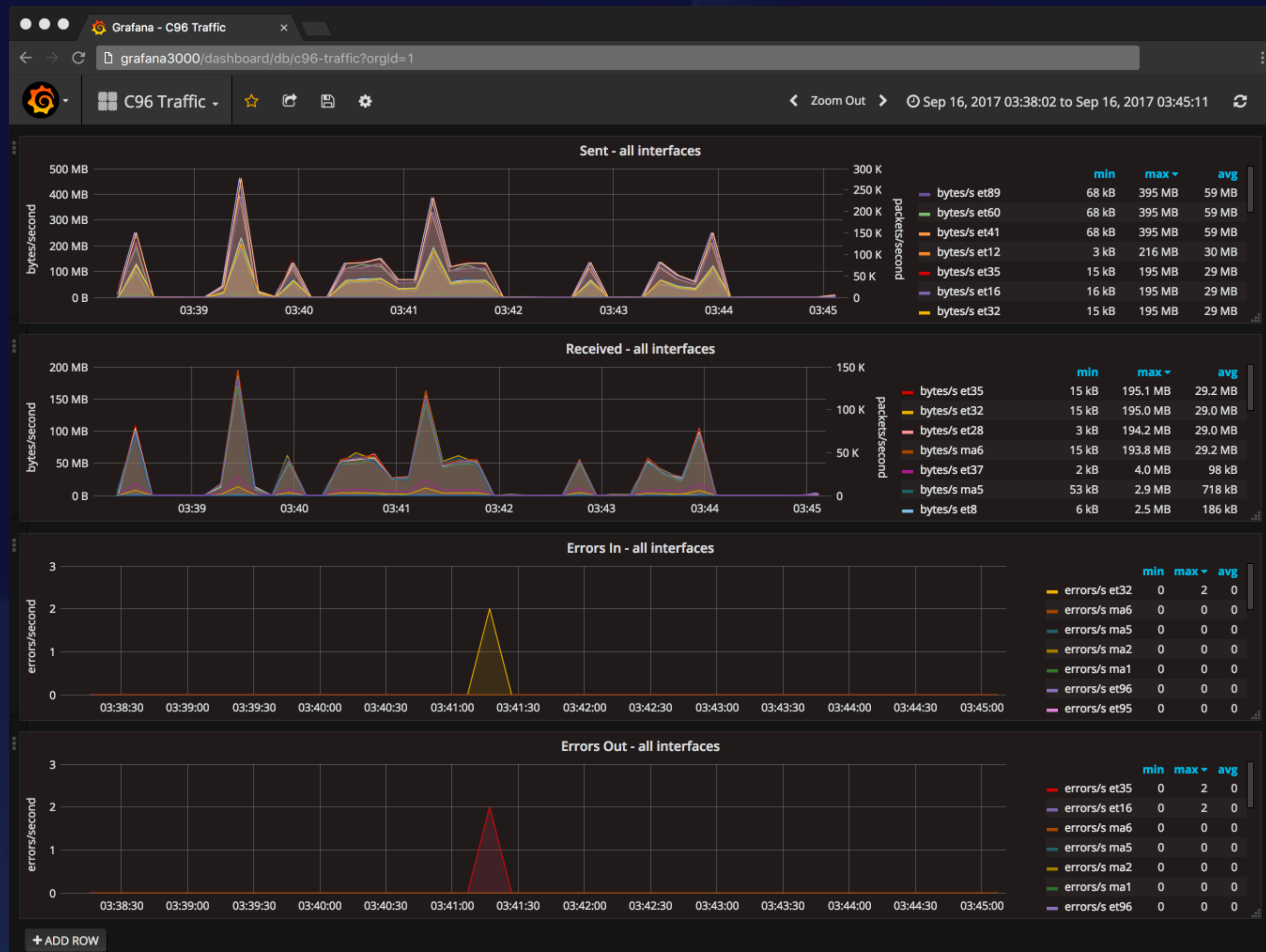
Accessible in real-time via Web Apps e.g.

- Grafana
- Chronograf



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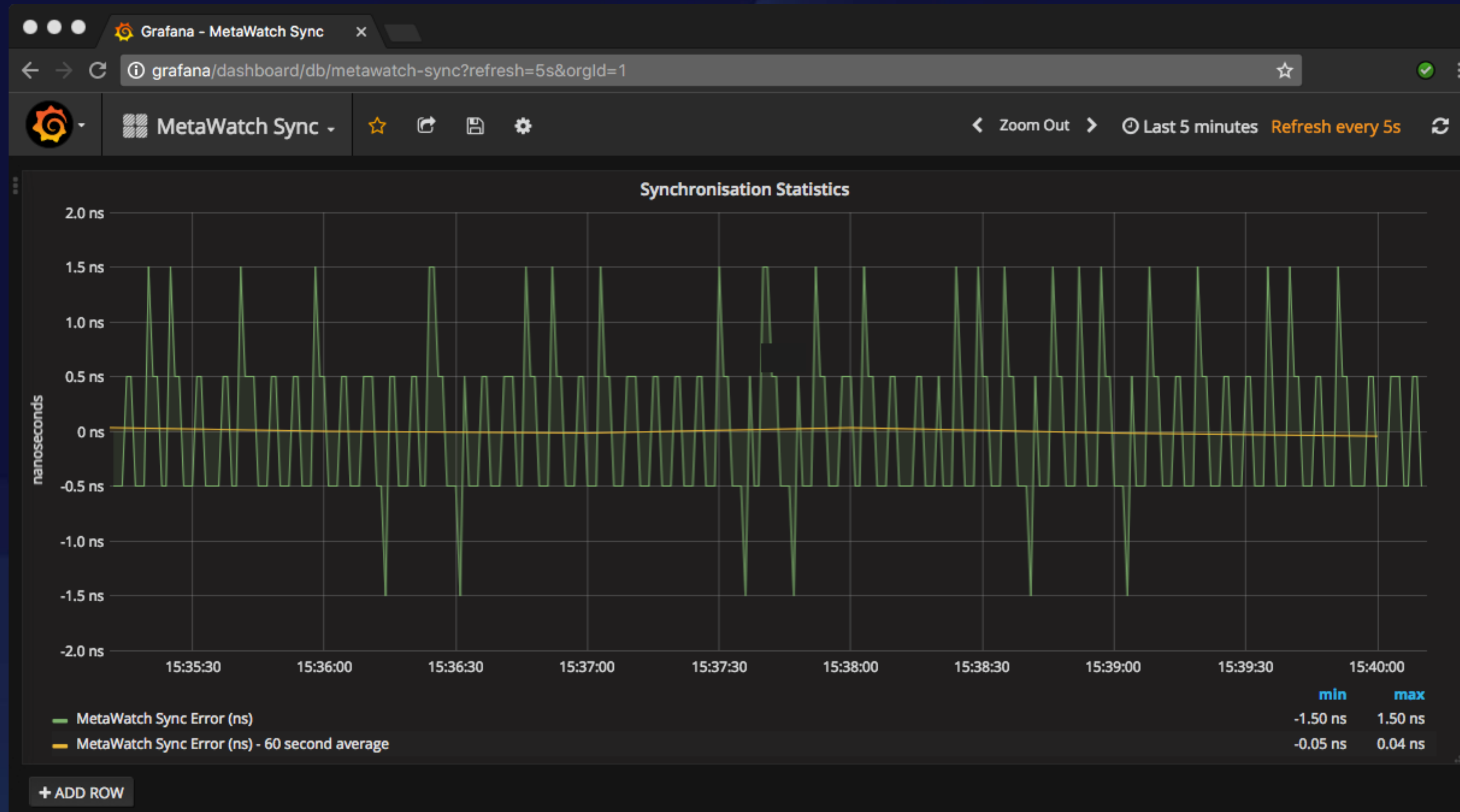
Telemetry: L1+ Port Counters





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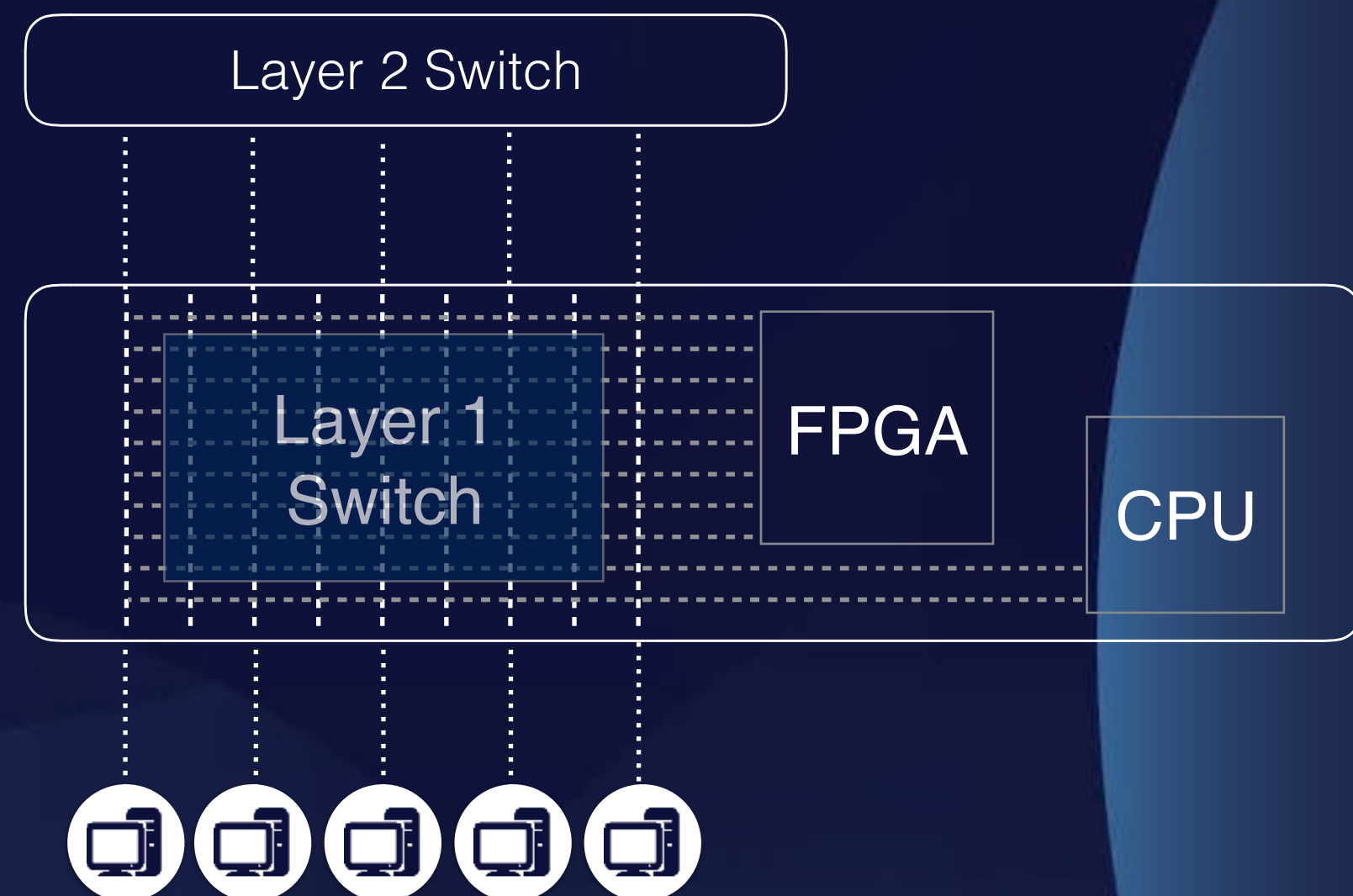
Telemetry: MetaWatch time sync





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Metamako as an Application Platform



Layer 1 Switch

- Any-to-any 1/10GbE connectivity
- Any-to-any replication
- Same latency as 1 m of patch cable/fibre
- Up to 96-external ports

FPGA

- Connected to the Layer 1 Switch with up to 76 x 1/10GbE ports
- Both Xilinx and Intel (Altera) options available including Xilinx UltraScale/UltraScale+
- Development Toolkit Available

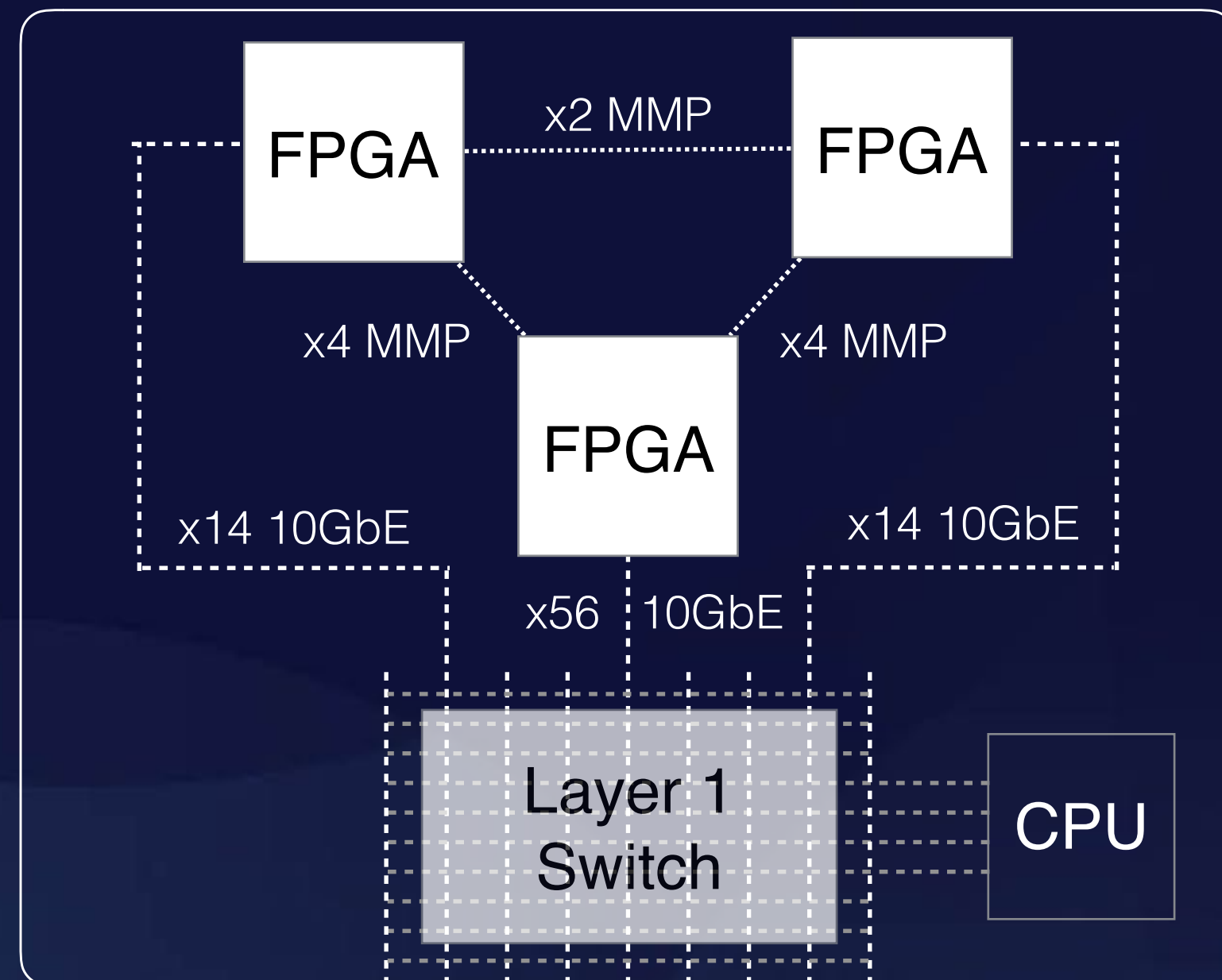
Management Processor (CPU)

- Running x86_64 Linux
- Connected to the Layer 1 Switch with up to 4 1/10GbE ports
- Supports LXC and Docker
- Provides Telegraf/InfluxDB/Kapacitor



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Now with 3 FPGAs in 1 or 2 RU



1 or 2 RU Chassis

Advantages

- 3 FPGAs in 1 or 2 RU
- Introducing MM Parallel Bus (MMP)
 - Latency-optimised bidirectional 32-bit data bus

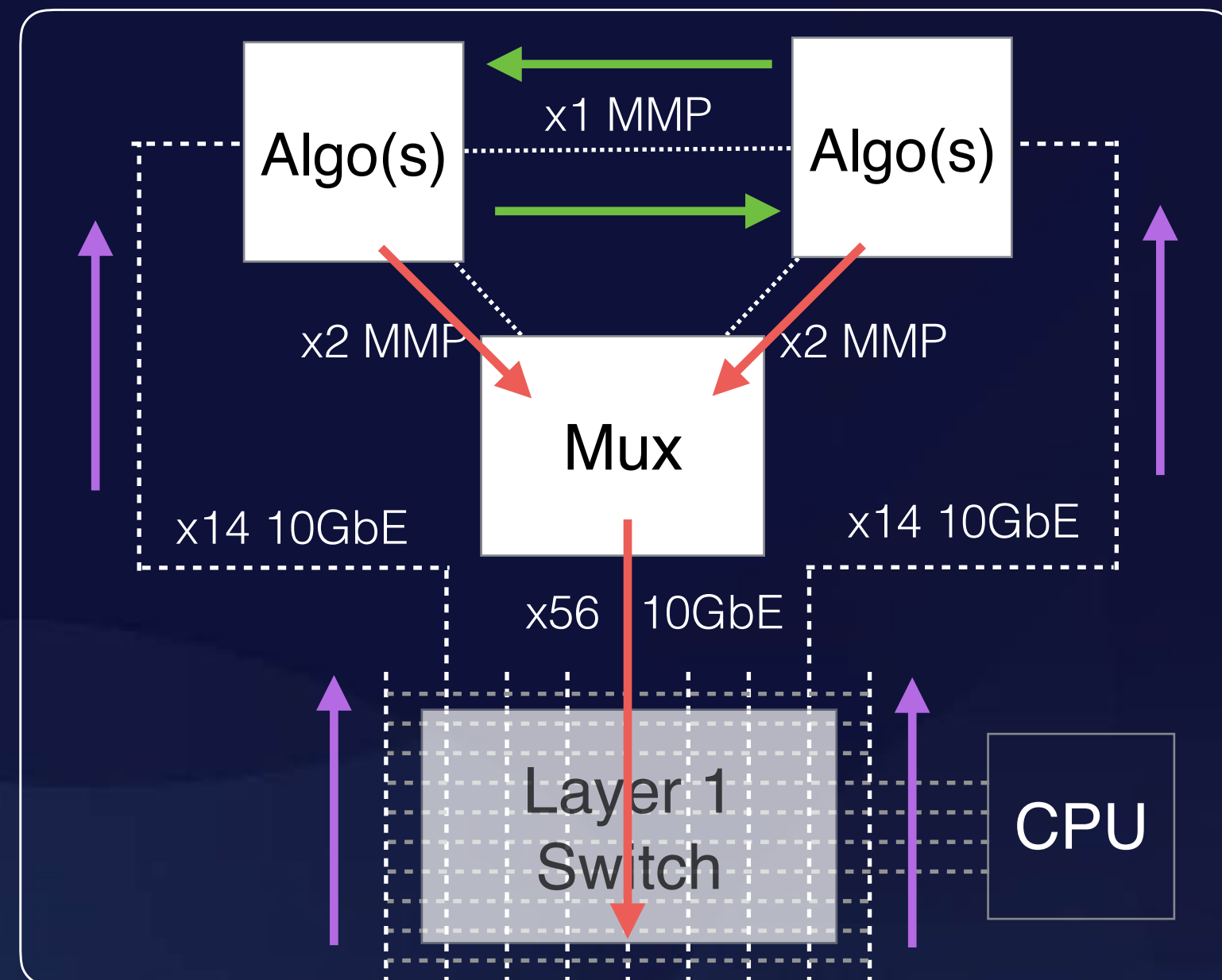
Architecture

- Central FPGA connected to each leaf FPGA with 2 MMP Busses
- Leaf FPGAs connected to each other with 1 MMP Bus
- Xilinx UltraScale/UltraScale+
- Connected to the Layer 1 Switch with up to 76 x 1/10GbE ports
- FPGA Development Kit available



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One way of leveraging them for trading



Advantages

- 3 beefy FPGAs all connected with MM Parallel Busses (MMP) allow for bigger/more algo instances

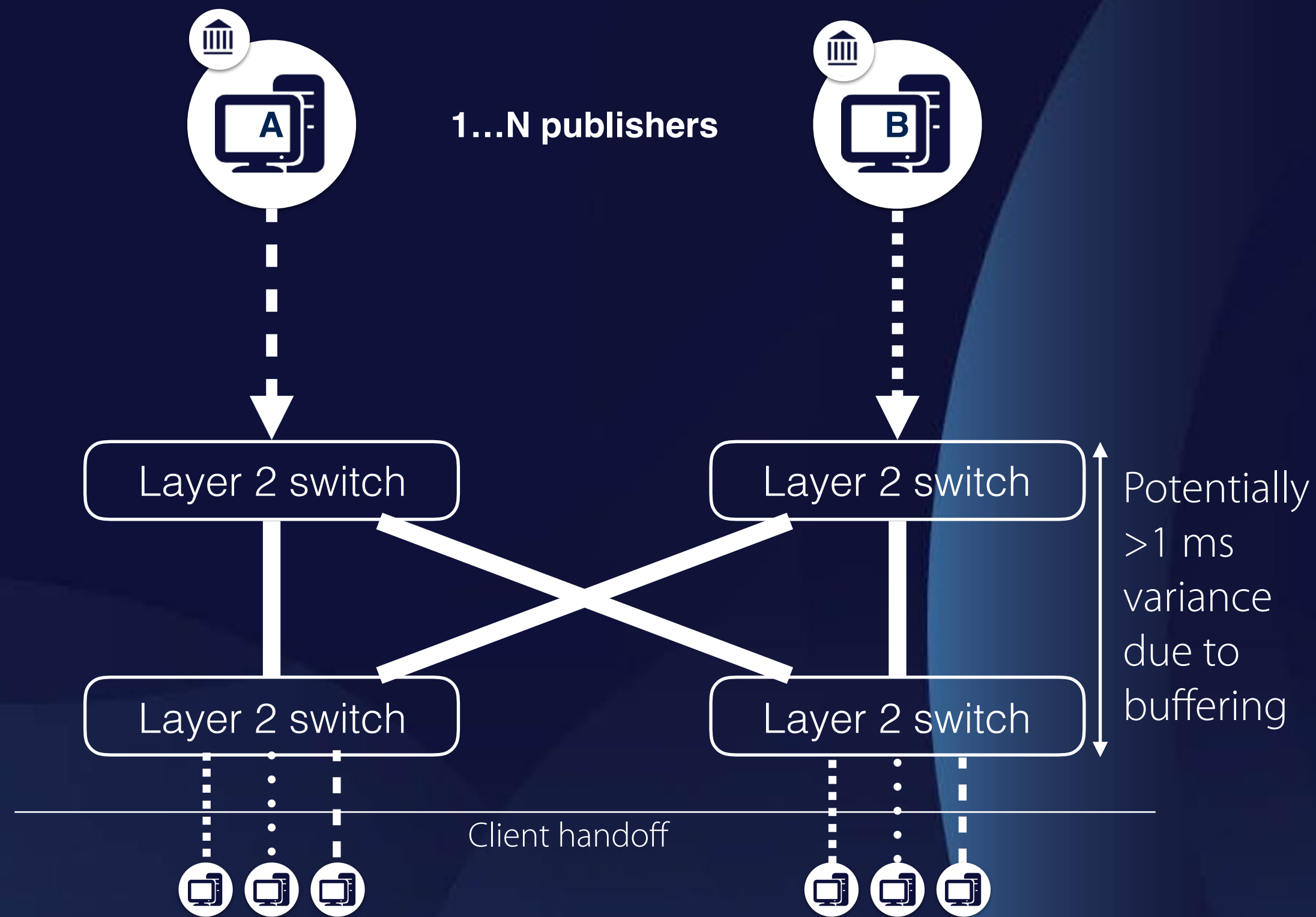
Leveraging internal interconnects

- Market data distributed to all 3 FPGAs via Layer 1 switch
- Algo(s) can be split across leaf FPGAs taking advantage of MMP busses
- Orders from leaf FPGAs into central FPGA Mux via MMP busses saving 10s of ns vs. between multiple devices



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The challenges of fair Market Data Distribution



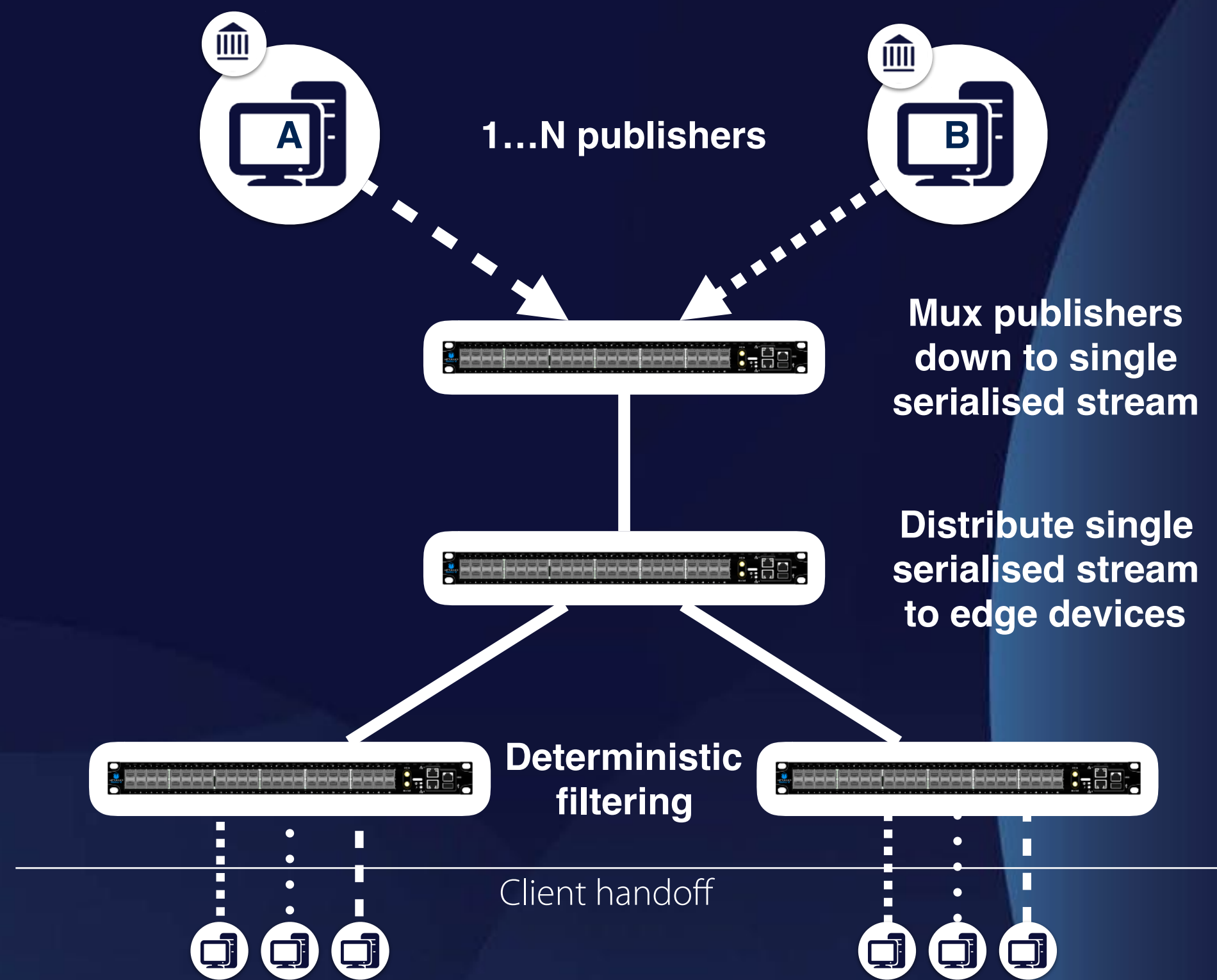
- Redundancy and simultaneous delivery are competing forces
- Latency can vary between each end client handoff based on
 - Load
 - Redundancy path
- Different clients want different subsets of data
- No frames can afford be dropped

With <1 us tick-to-trade, >1 ms variance can have a significant impact on clients



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Fair Market Data Distribution



Architecture

- Three deterministic tiers:
 1. Mux
 2. Replicate
 3. Filter

Advantages

- Guarantee-able fairness
- Can easily be made redundant
- At the filtering/client distribution tier:
 - Filter the subset of feeds needed for each client connection (IGMP) — standard client interface
 - Black-list or white-list multicast groups available to clients on a per-port basis



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