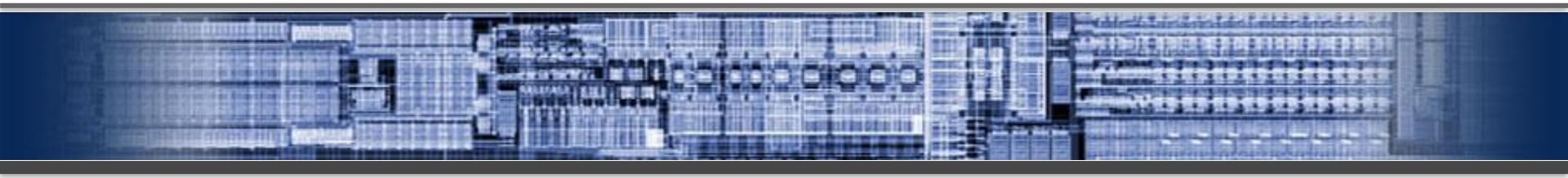
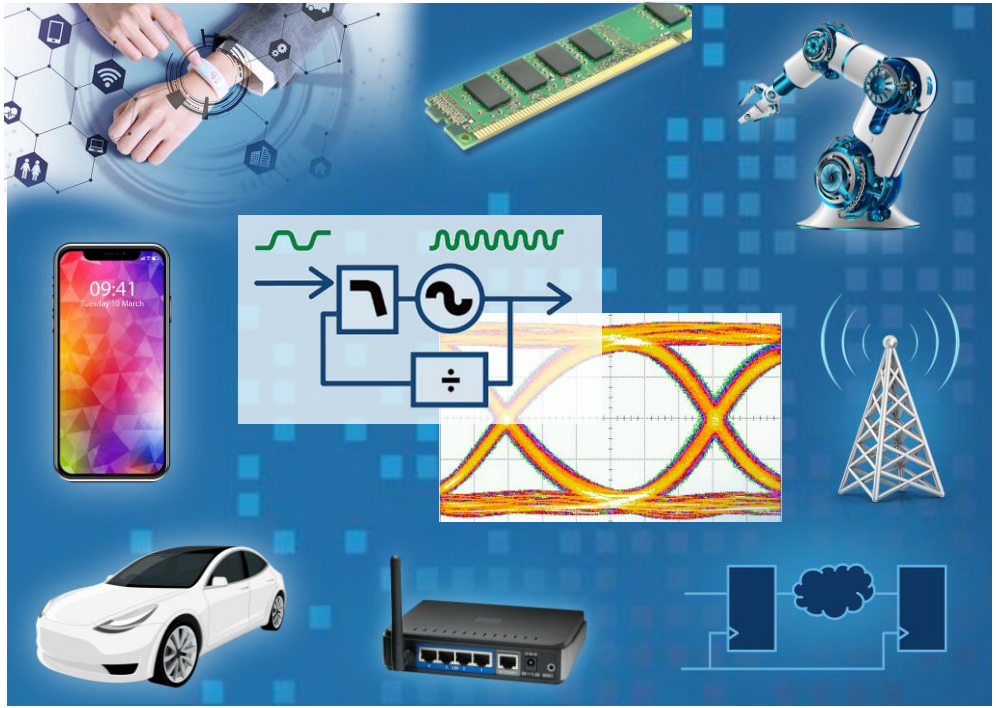


10GbE and 25GbE Low-latency SerDes PMAs for ASIC Implementation

Jeff Lumish & Jeff Galloway

Silicon Creations Overview

- Mixed Signal Silicon IP provider for ASICs: SerDes, PLLs, and Oscillators
- Design Centers: Atlanta, USA and Krakow, Poland
- 5-time TSMC “Analog Mixed-Signal Partner of the Year” (2017 – 2021)
- ISO9001 certified
- Proven/Production IPs from 3nm to 180nm
- Hundreds of successful customers including more than 5 in HFT



Multiprotocol PMA portfolio

Ported to...

Data rate/lane (Gbps) ----->

0.1 1.0 1.2 2.0 2.5 3.1 4.0 5.0 6.2 8.1 10 12.5 16 20 26 28 32

GF40LP
TSMC 40 LP, 40G ✓ LL
UMC 28 HLP
TSMC 28 HPC+
TSMC 12FFC/16FFC ✓ LL
TSMC 6/7FF, GF12LP+

Processes from 40LP to 12FF and 6FF

Very wide, continuous data rate operation

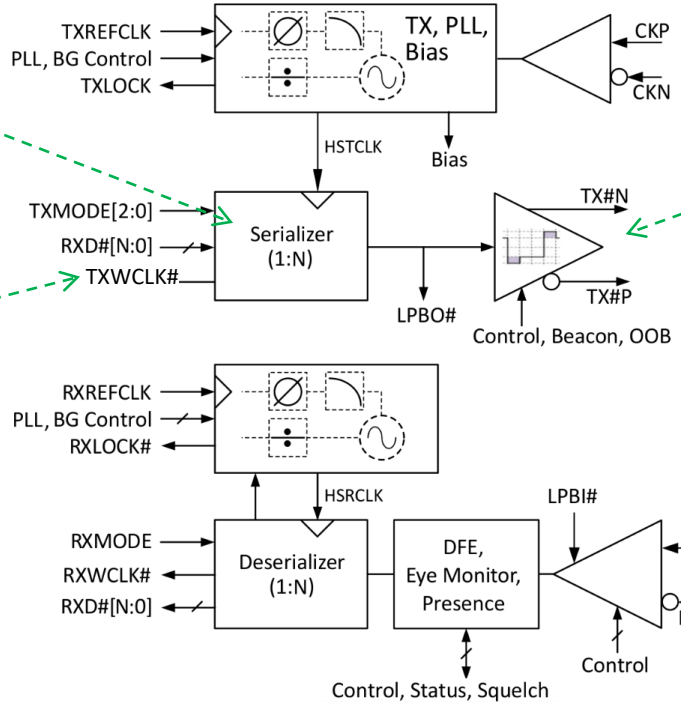
- V-by-One HS
- IEEE 802.3 1GBASE-X, SGMII, QSGMII
- XAUI IEEE 802.3 10GBASE-X, RXAUI
- JESD204B LV-OIF-6G-SR, LR
- USB3.2 – Gen1, Gen2 – X1, X2
- IEEE 802.3 10GBASE-R, 10GBASE-KR, XFI
- OTU1, OTU2, OTU2e
- SATA/SAS 1 – 3, SAS6, SAS12
- SMPTE SDI-SD/HD/3GHD, 6G-SDI, 12G-SDI
- HDMI 2.1 (with AC coupling)
- JESD204B/C LV-OIF-11G-SR, MR
- CPRI Rates 1 – 9
- HiGig, HiGig+, HiGig2, …
- Fiber Channel 1G – 16G
- V-by-One US
- Display Port 1,2, 1.3, 2.0, eDP 1.3, 1.4
- SRIO
- 100G-KR4
- Interlaken
- PCI-Express Gen 1 to 5 (+CCIX, CXL)
- OIF-CEI-28G-SR, MR, JESD204C, CPRI

Supporting >20 protocols Incl. 10GbE, 25GbE, PCIe3/4/5

Low-latency SerDes PMA

Ser/Des width can be custom
(E.g. 8b, 22b, to match MAC)

Programmable clock phase
for system latency reduction



Tx Load to 1st bit out
latency < 5UI
= 0.49ns @ 10.3Gbps

Rx last bit in to parallel
out latency < 8UI
= 0.77ns @ 10.3Gbps

Note : Latency specifications are not STAC benchmarks

Business model

- License fee per Design Chip developed; win-win discounts for subsequent chips
- Accurate simulation models for system and latency verification
- Collaboration with ASIC design service companies fully supported
- License includes two years of unlimited support for SerDes/PLL IP integration into the chip, chip bring-up and debug
- Mark and return your Response Card for more information!