STAC Update for Fast Data

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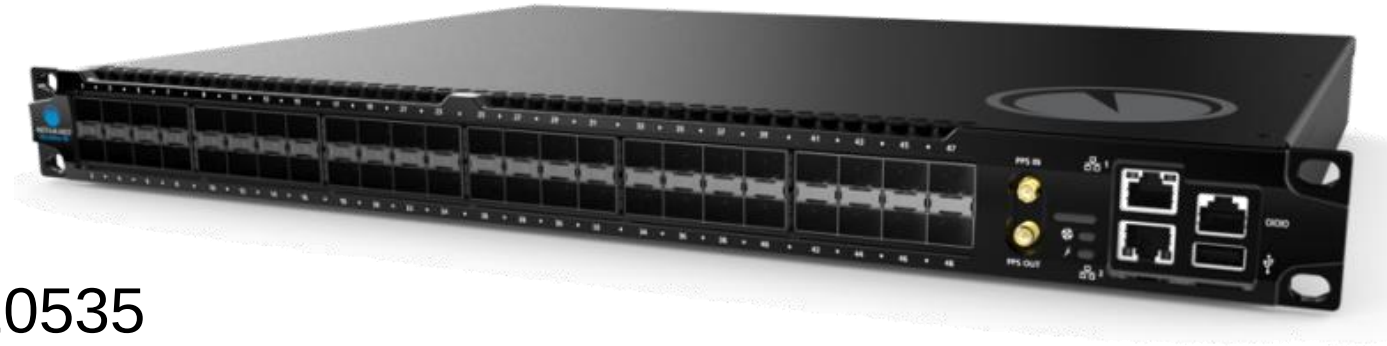
New STAC-TS results (in the STAC Vault)

- 2 x Arista DCS-7130-48L
  - MetaWatch 0.11.0beta1 firmware
  - MOS-0.23.1 with
- Arista SFP-10G-SR SFP+
- TimeTech Pulse Distribution Unit 10535
- Intra-device port-sync error (STAC-TS.PSE1)
- Inter-device port-sync error (STAC-TS.PSE2)



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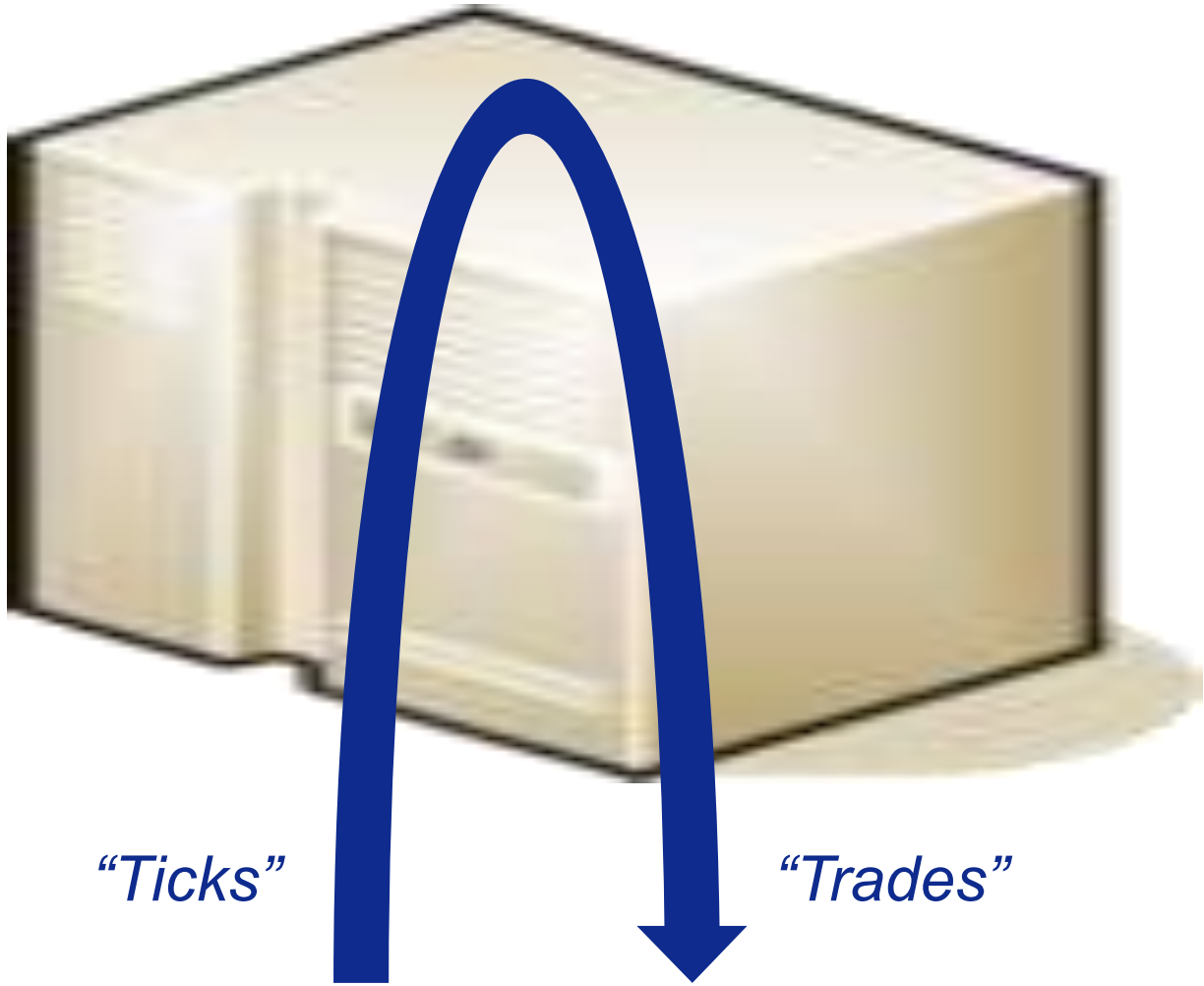
STAC-T0 vs STAC-T1

- Both are a tick-to-trade pattern
  - UDP in
  - TCP out
- Both use wire timestamps
  - High accuracy
  - Work with any trading platform (sw/hw)
- STAC-T1 includes protocol handling
  - Market data decoding
  - Order encoding
- STAC-T0 does not
  - No market-specific logic
  - Isolates network I/O latency



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Quick review: Latest STAC-T0 results

- Finalized and published Exablaze STAC-T0 results
  - Refined the calculation of inferred timestamps (sub-ns impact)
  - Matt Grosvenor will describe some of the complexities shortly
- New high ingress rates tested:
  - 1.9 M packets/sec (7.7 Gbps) for 507B frames
  - 11 million packets/sec (6.2 Gbps) for 68B frames
- Set new records in every measurement
  - Over 50% lower latency than previous records

www.STACresearch.com/EXA181106

Across all message sizes and all message rates, Actionable Latency:

- Max of ~44 nanoseconds (STAC-T0.β1.*.*.ACTIONABLE.MAX)
- Min of ~31 nanoseconds (STAC-T0.β1.*.*.ACTIONABLE.MIN)

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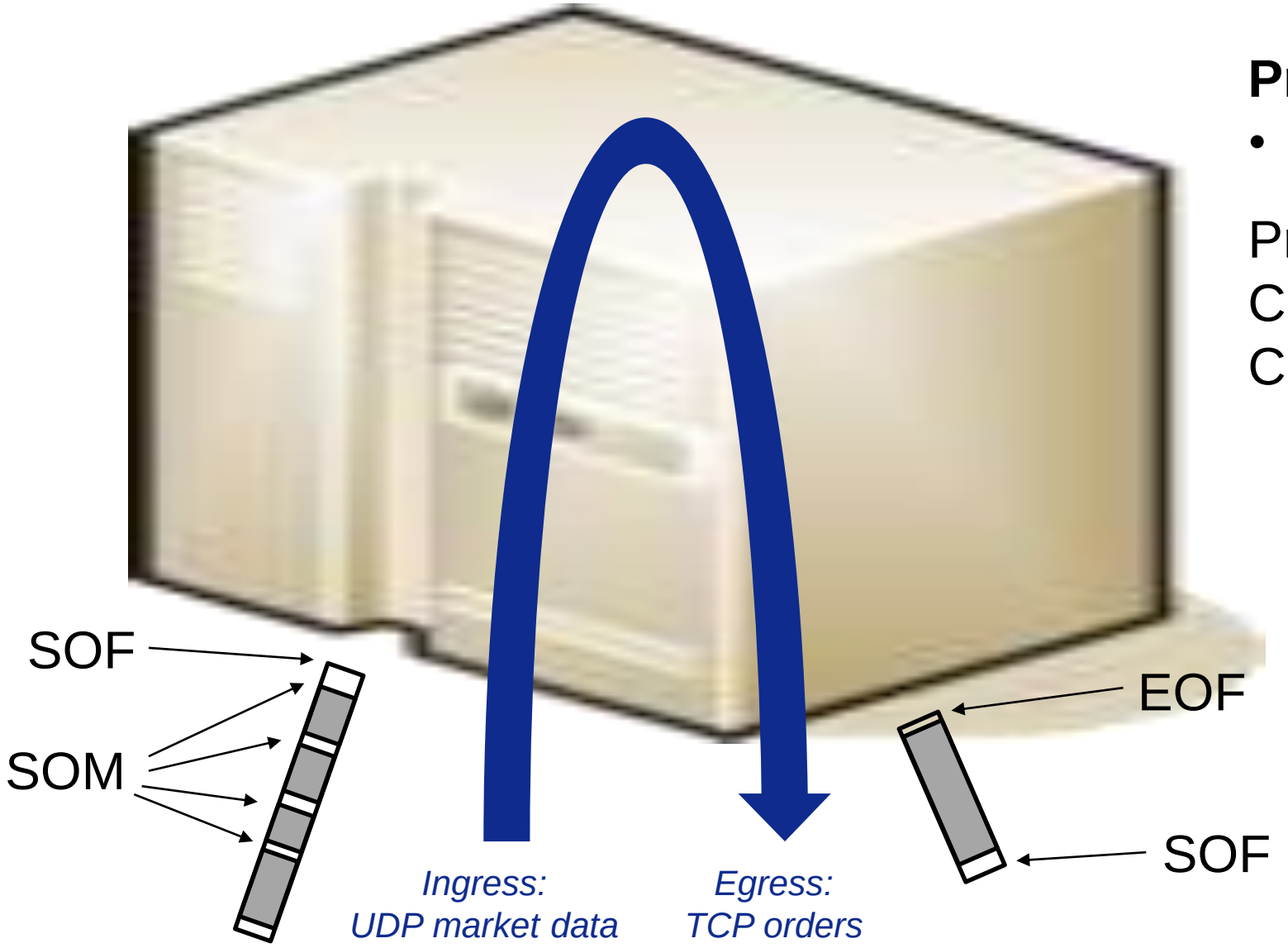
Exegy under STAC-T1.EMINI

- Tested Exegy Xero 1.0.3 for CME Tick-to-Trade Execution
  - FPGA card
- First we had to bring STAC-T1.EMINI up to date
  - Updated to latest CME market data protocol (MDP 3.0)
  - Dataset is now a recent quadruple witching day
  - Increased the set of latencies reported
- Because market data is different, these results cannot be fairly compared to previous STAC-T1 results

Latencies



Previous STAC-T1.EMINI:

- SOF(in) to EOF(out)

Pro: complete latency picture
Con: includes serialization delay
Con: not useful for algos that wait for mkt data messages

Updated STAC-T1.EMINI:

Above, plus –

- SOF(in) to SOF(out)
- SOM(in) to SOF(out)
- SOM(in) to EOF(out)

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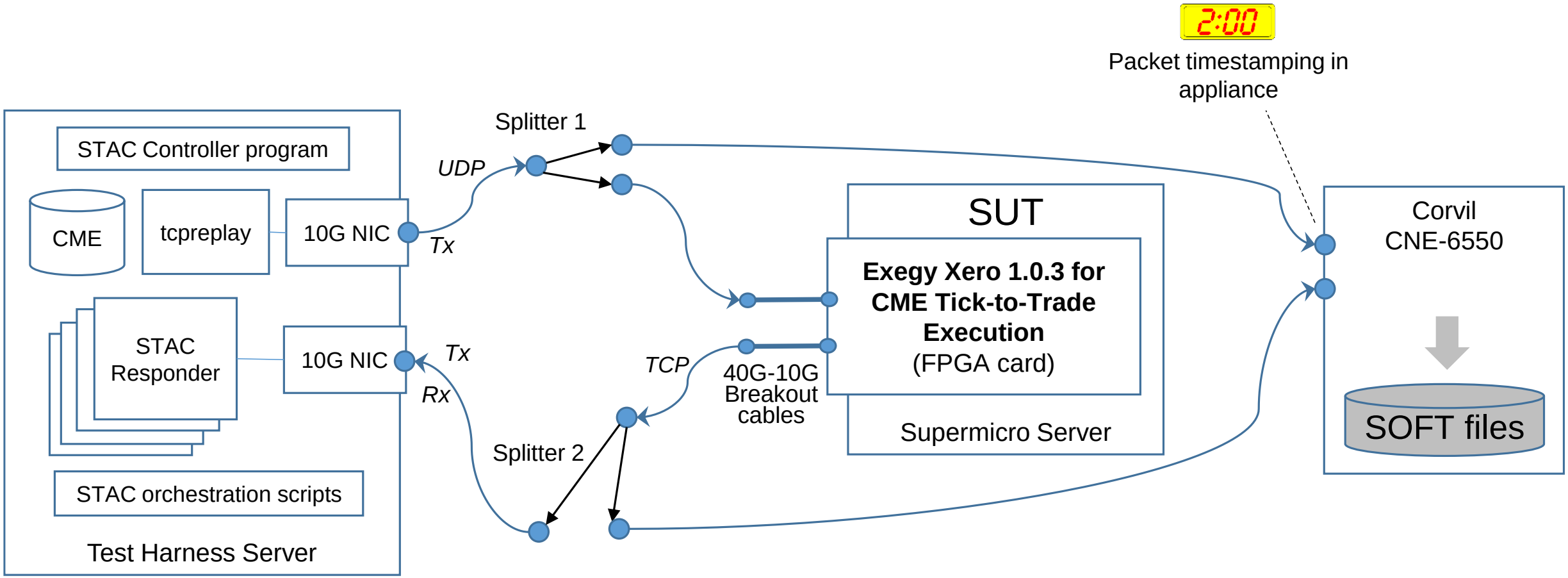
Test setup



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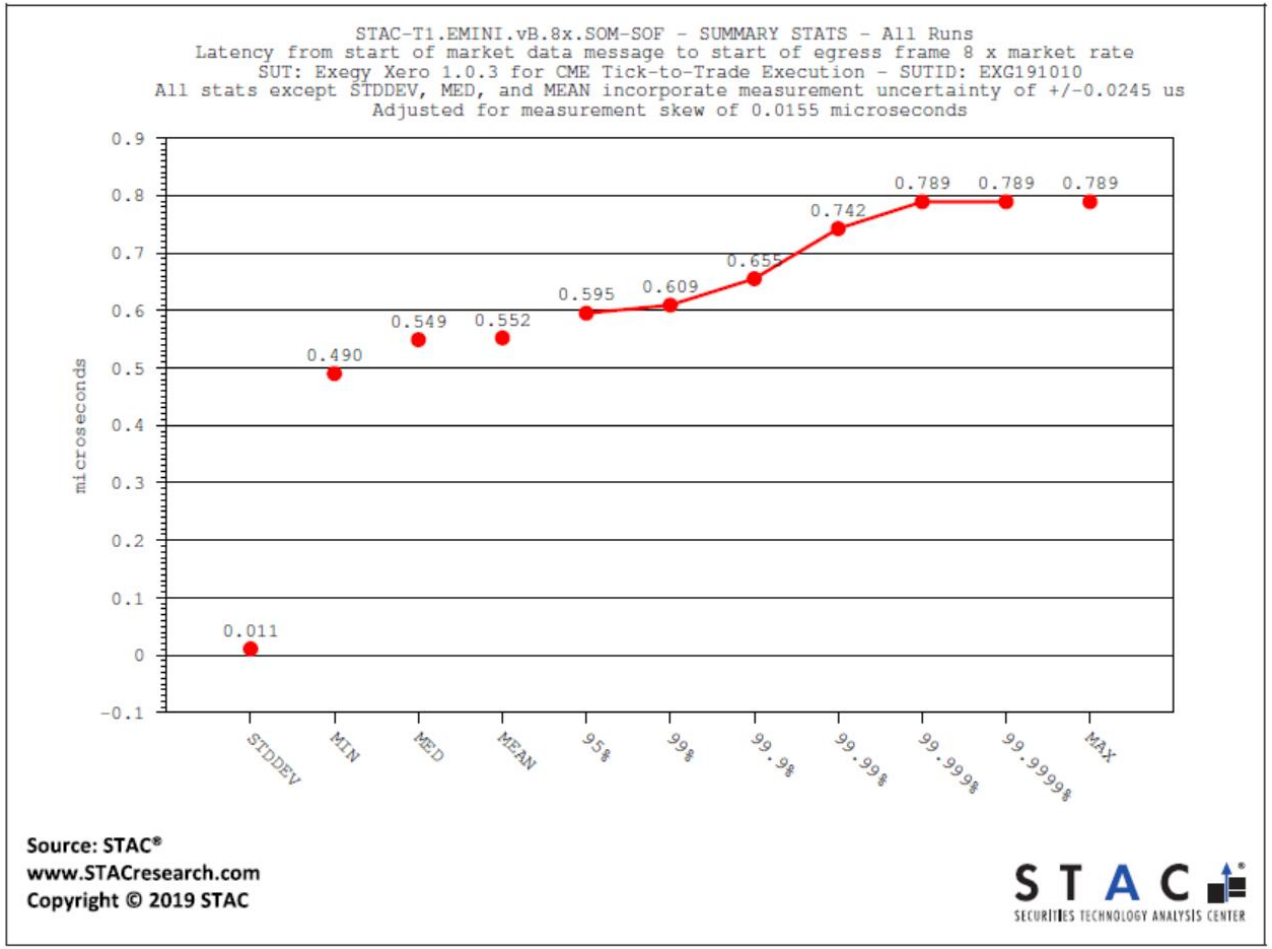
Results highlights

STAC-T1.EMINI.vB.1x.SOM-to-SOF

STAC-T1.EMINI.vB.8x.SOM-to-SOF

At both 1x and 8x market rate, the latency from the start of the market data message to the start of the order frame was:

- 0.552 microseconds (MEAN)
- 0.609 microseconds (99P)
- 0.789 microseconds (MAX)
- 0.011 microseconds (STDEV)



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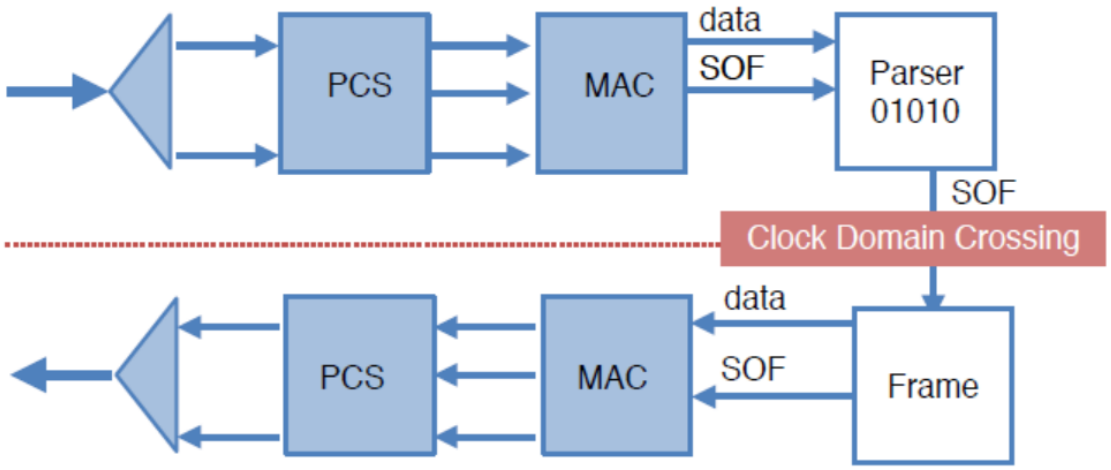
“STAC MAC”

- Business context: There’s a market for MAC/PHY IP cores
- Purpose of the benchmark: measure the performance of vendor-provided MAC and PHY for a given FPGA chip
- Started with a proposal from Matt Grosvenor (Exablaze): www.STACresearch.com/STAC-Summit-13-Jun-2018-exablaze
- Olivier Baetz developed a very detailed proposal



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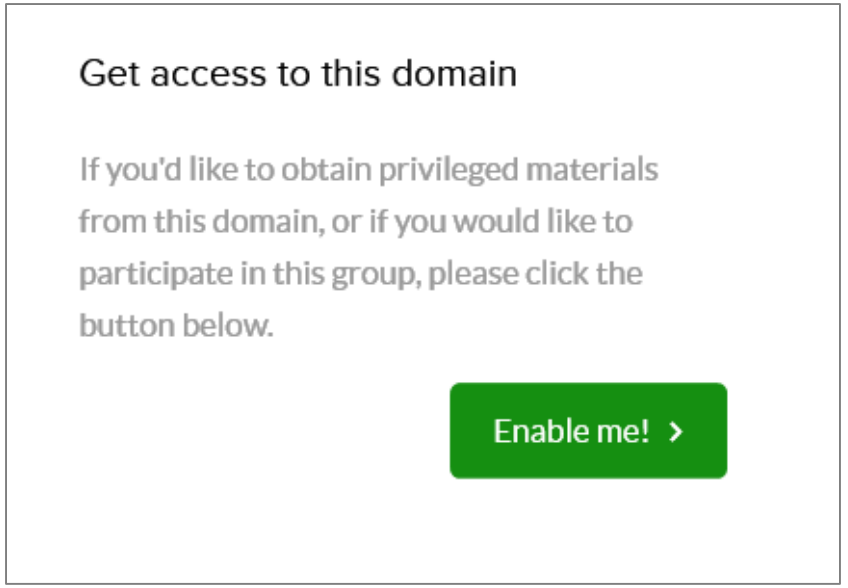
“STAC MAC” continued

- Has gotten a lot of valuable discussion in the STAC online forums
- Have crystallized the key debating points
- Debate to happen by telecon this quarter
- Sign up to be involved: www.STACresearch.com/nio



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