Accelerating Applications with the Xilinx Quantitative Finance Library

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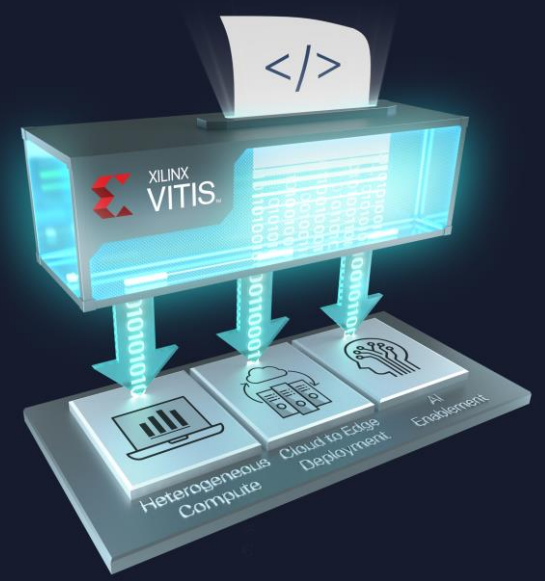
Nov 2019

XILINX.

Vitis Software Platform and Alveo Cards.

XILINX VITIS™

- Standards, Open

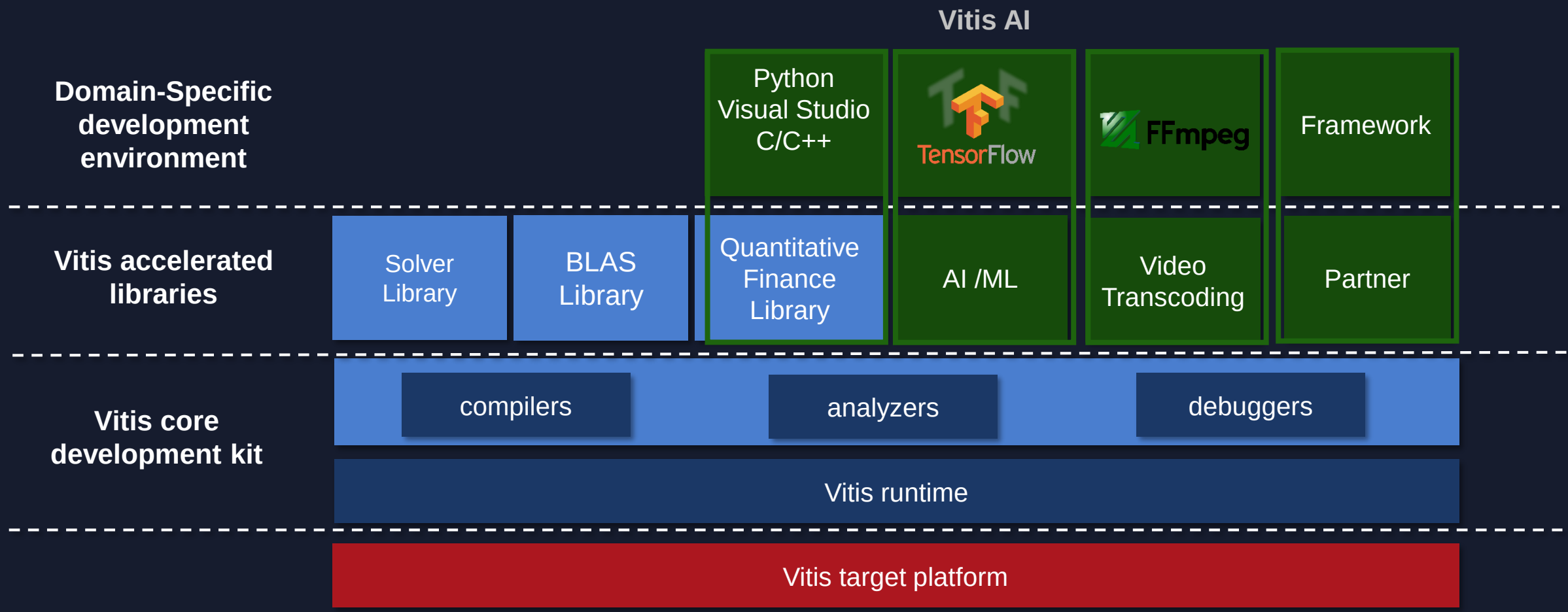


XILINX ALVEO™

- Acceleration Cards

XILINX

Vitis: Unified Software Platform



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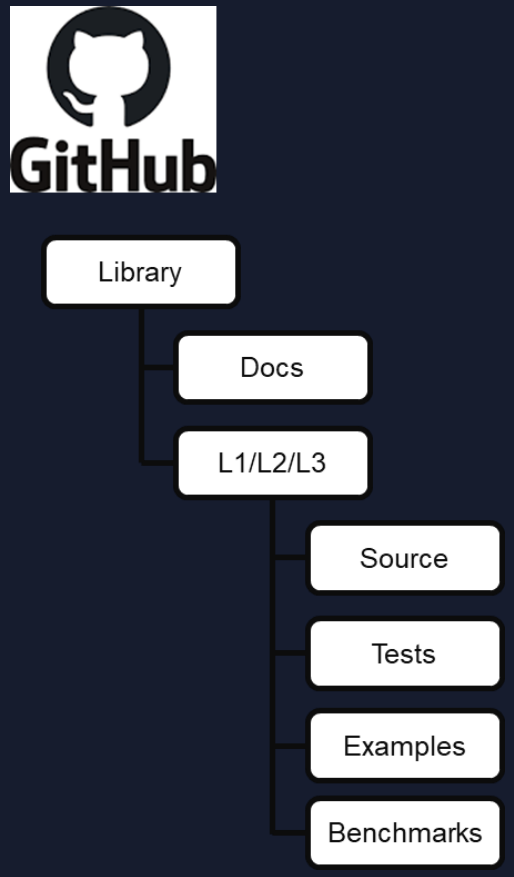
Vitis Accelerated Libraries



XILINX Developers Support

Vitis Quantitative Finance Library

2019.2

Search docs

LIBRARY OVERVIEW

- Requirements
- License
- Trademark Notice
- Release Note

USER GUIDE

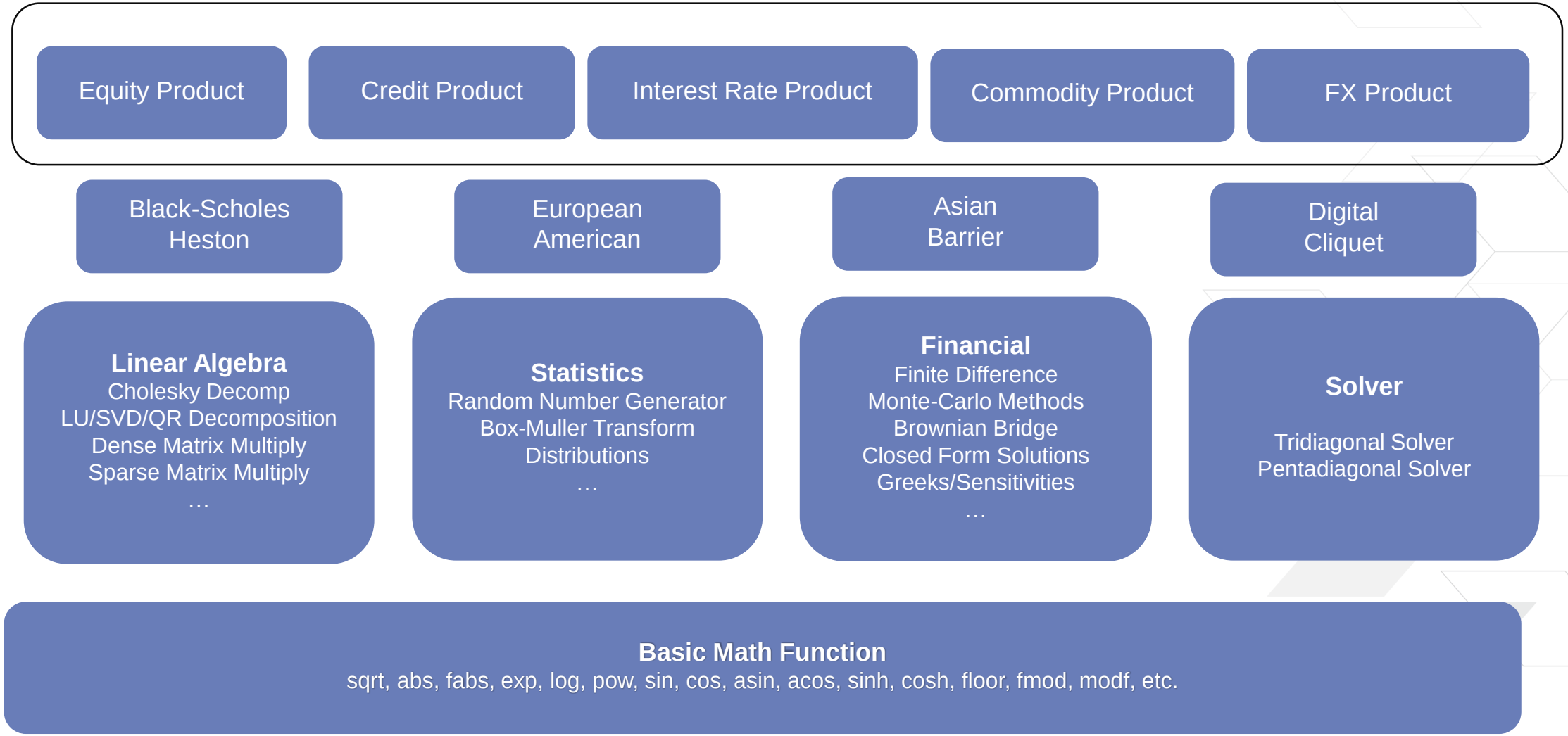
- Pricing Models and Numerical Methods
- L1 Module User Guide
- L2 Kernel User Guide
  - Pricing Engine Overview
  - Pricing Engine Kernel Design
  - Pricing Engine Kernel APIs
  - Pricing Engines Demo
  - Other Engine Kernel Design
- L3 Overlay User Guide

» L2 Kernel User Guide

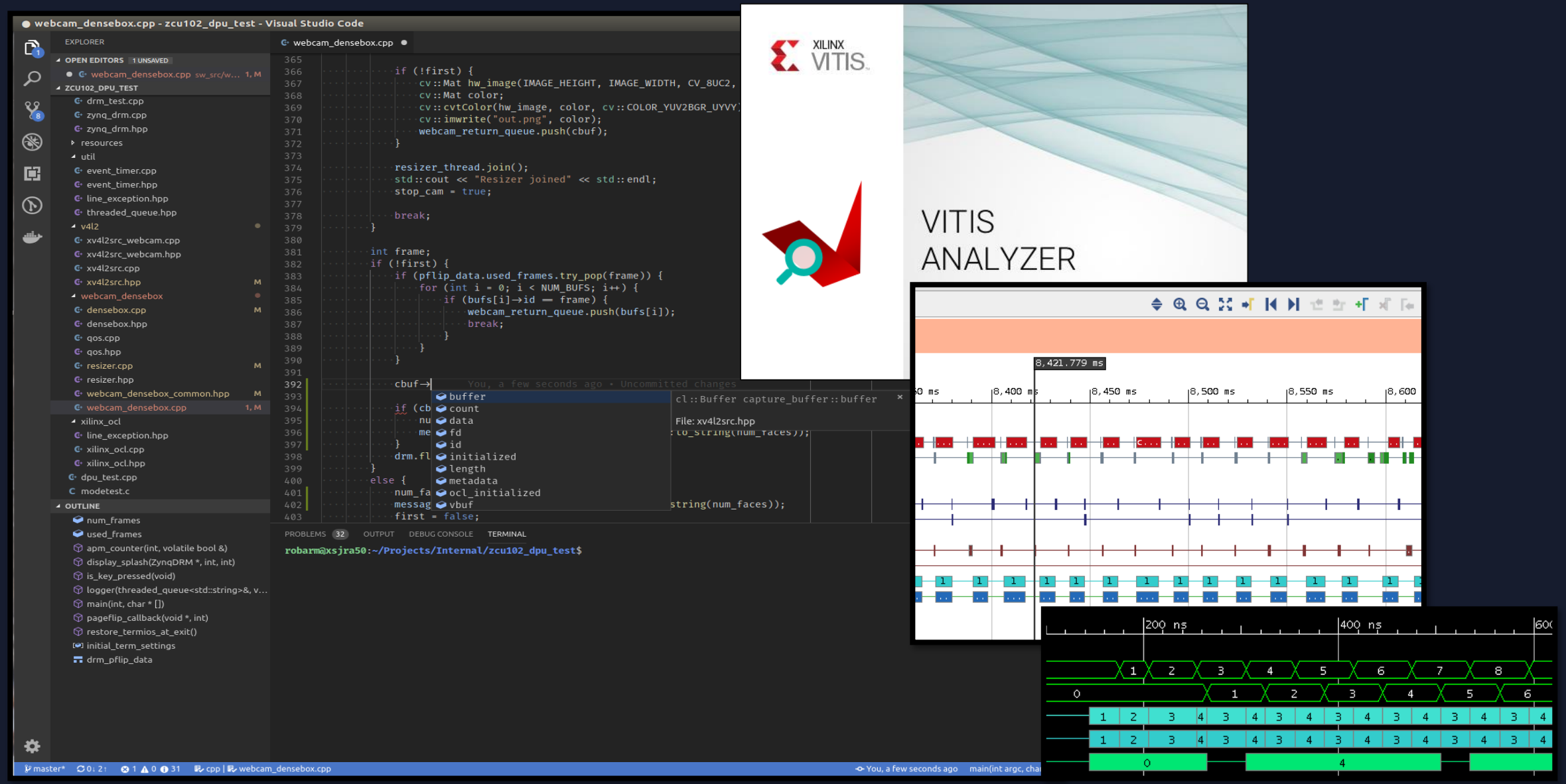
L2 Kernel User Guide

- Pricing Engine Overview
- Pricing Engine Kernel Design
  - Internal Design of MCEuropeanEngine
  - Internal Design of MCEuropeanHestonEngine
  - Internal Design of Asian Option Pricing Engine
  - Internal Design of Digital Option Pricing Engines
  - Internal Design of Barrier Option Pricing Engine
  - Internal Design of Cliquet Option Pricing Engine
  - Internal Design of American Option Pricing Engine
  - Internal Design of MCMultiAssetEuropeanHestonEngine
  - Internal Design of MCHullWhiteCapFloorEngine
  - Internal Design of MCEuropeanHestonGreeksEngine
  - Internal Design of Closed Form Black-Scholes-Merton
  - Internal Design of Closed Form Heston
  - Internal Design of Closed Form Merton 76
  - Internal Design of Garman Kohlhagen
  - Internal Design of Quanto
  - Internal Design of Cox-Ross-Rubinstein Binomial Tree
  - Internal Design of Finite-Difference Hull-White Bermudan Swaption Pricing Engine

Xilinx VITIS Quantitative Finance Library



Vitis -- Familiar SW Environment



Alveo U50 – Low Profile Acceleration Card

Fintech

Storage

Machine Learning

Database

Card	Alveo U50
Primary Application	Fintech + Storage + Database + ML
FPGA Design	XCU50
CCIX	Yes
Device VCCINT	0.85V
Width	Single slot
Form Factor (Passive)	HHHL
Memory Target	8 GB HBM
Memory Config	Dual Stack, 32 pseudo-ports
PCIe	2x Gen4x8, 1x Gen4x8, Gen3x16, CCIX
Network I/F	2x SFP- DD* or 1X QSFP28
Thermal	Passive
Power (Max TDP)	75W
KLuts	872K

* During ES, U50 card will have 2 SFP-DD ports

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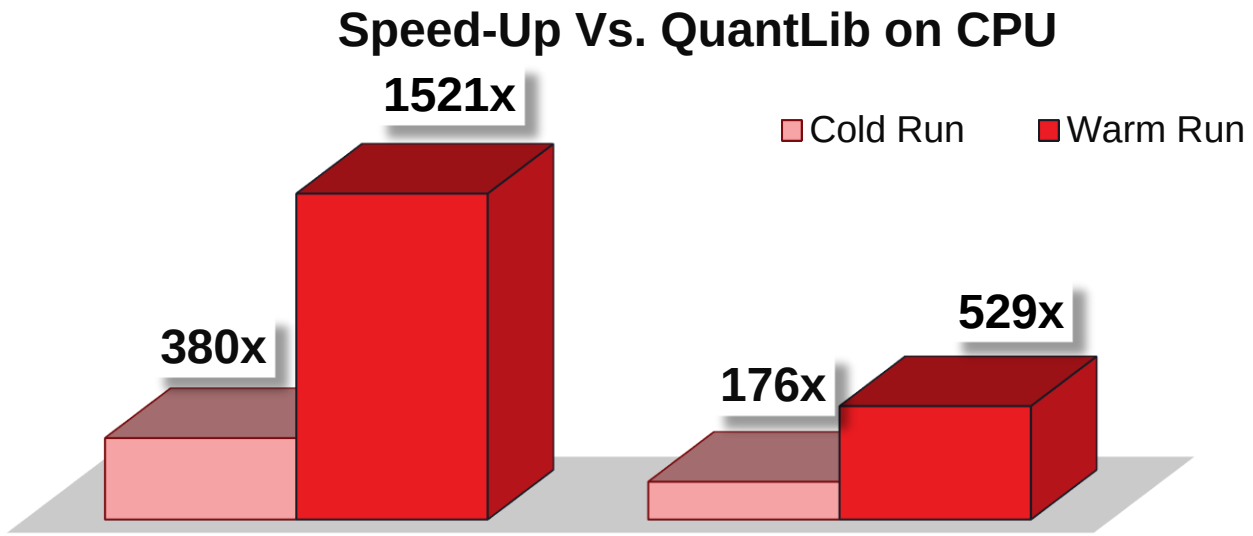
Quantitative Finance Library (NON-STAC Benchmark)



Monte Carlo European Options Pricing		
	Cold Run	Warm Run
QuantLib	20.155 ms	20.155 ms
Vitis Quantitative Finance Library	0.053 ms	0.01325 ms
Speed-Up	380X	1521X

Monte Carlo American Options Pricing		
	Cold Run	Warm Run
QuantLib	1038.105 ms	1038.105 ms
Vitis Quantitative Finance Library	5.87 ms	1.96 ms
Speed-Up	176X	529X

CPU : 2 Intel(R) Xeon(R) CPU E5-2690 v4 @3.20GHz, 8 cores per processor and 2 threads per core.
Xilinx : Vitis Quantitative Finance Library v1.0 running on 1 Alveo U250
Cold Run: Pricing Engine starts up in response to a request.
Warm Run: Pricing Engine is already running, with sufficient memory allocated to handle the request

Adaptable.
Intelligent.

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