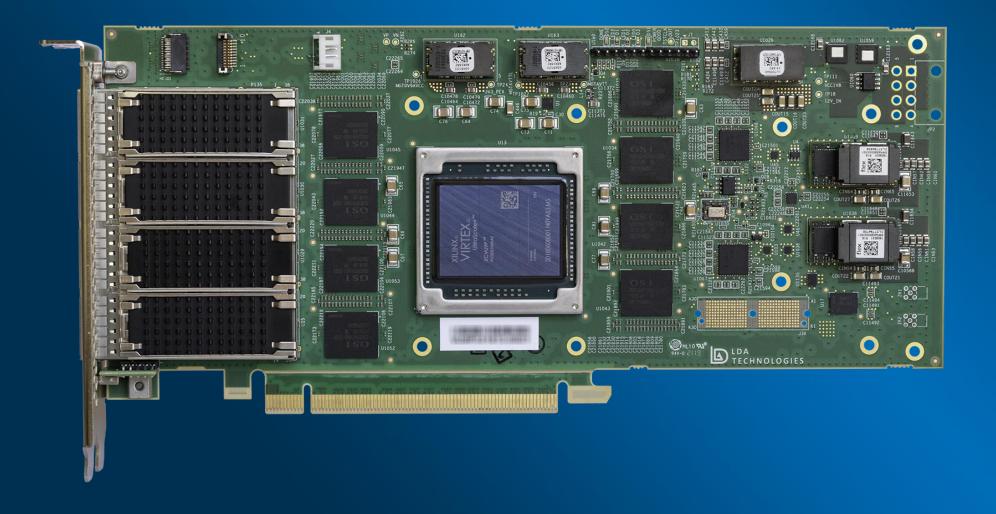
## WINNING THE RACE 17/11/2/27 ULTRA-LOW LATENCY WITH LDA



Providing FPGA-based solutions for ultra-low latency markets since 2010





FPGA board tailored for ultra-low latency applications

 8 independent banks of static memory Total: 576 Mbytes

User logic to memory access latency
 Write: 9 ns | Read: 12 ns



## New generation of LDA FPGA board enclosures





Any FPGA board

• 48x 25 GbE ports

Up to Xeon Scalable 2nd Gen CPU

Up to 128 GB ECC DDR4 memory



Up to 4 NVME Drives

PCle x8 slot for an add-on card (NIC or a second FPGA board)

Optional equalized latency across all 48 ports: < 150 ps variance\*</li>

Optional L1 fabric: 2 ns port to port



## LDA 16-bit / 644 MHz 10G IP Cores

MAC / PCS

6.2\* ns roundtrip (+ 15.4 PMA)

• Over 40% boost vs. 32-bit / 322 MHz

FPGA IP Core News

• Over 15% boost vs. 20-bit / 515 MHz

\*Not STAC Benchmarks

Measured with LDA 30 ps accuracy latency measurement system



FPGA IP Core News

MUX

27.8\* ns

Layer 3 Router

45\* ns

\*Not STAC Benchmarks
Measured with LDA 30 ps accuracy latency measurement system



Tick-To-Trade Actionable I/O Latency

Min: 28\* ns

Max: 40\* ns

\*Not STAC Benchmarks

Measured with LDA 30 ps accuracy latency measurement system



## Thank You

