

A horizontal band across the top of the slide shows a close-up, blue-tinted image of a silicon wafer with a grid of square dies.

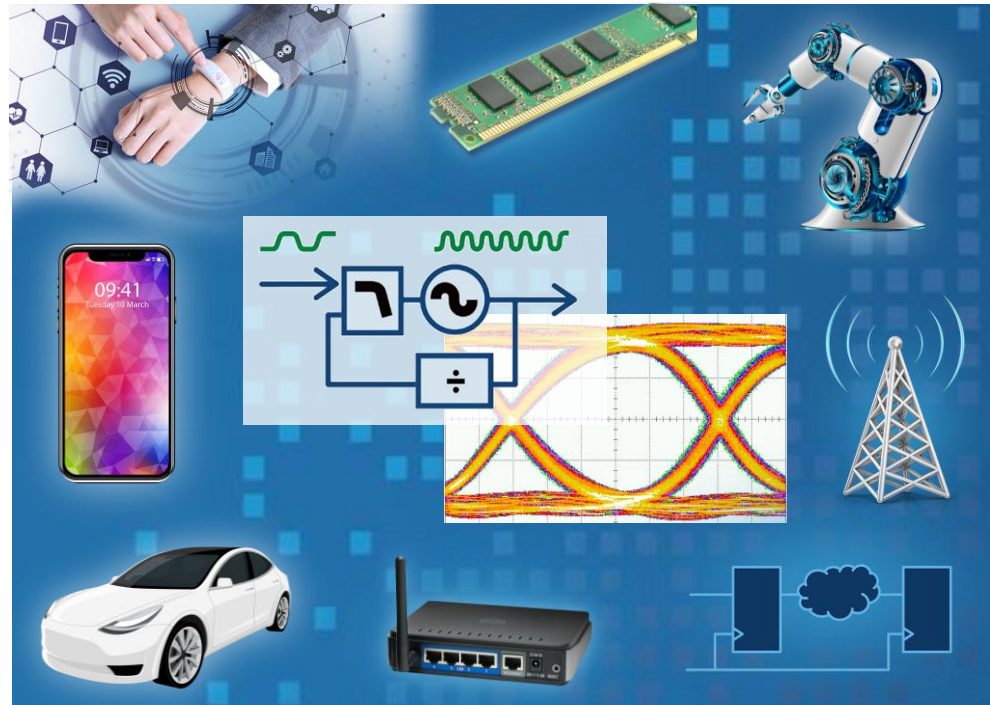
10GbE and 25GbE Low-latency SerDes PMAs for ASIC Implementation

Jeff Lumish & Jeff Galloway

Silicon Creations Overview



- Mixed Signal Silicon IP provider for ASICs: SerDes, PLLs, and Oscillators
- Design Centers: Atlanta, USA and Krakow, Poland
- 5-time TSMC “Analog Mixed-Signal Partner of the Year” (2017 – 2021)
- ISO9001 certified
- Proven/Production IPs from 3nm to 180nm
- Hundreds of successful customers including more than 5 in HFT



Multiprotocol PMA portfolio

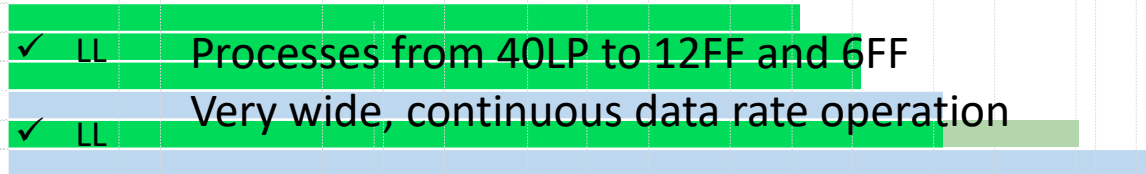


Ported to...

Data rate/lane (Gbps) ----->

0.1 1.0 1.2 2.0 2.5 3.1 4.0 5.0 6.2 8.1 10 12.5 16 20 26 28 32

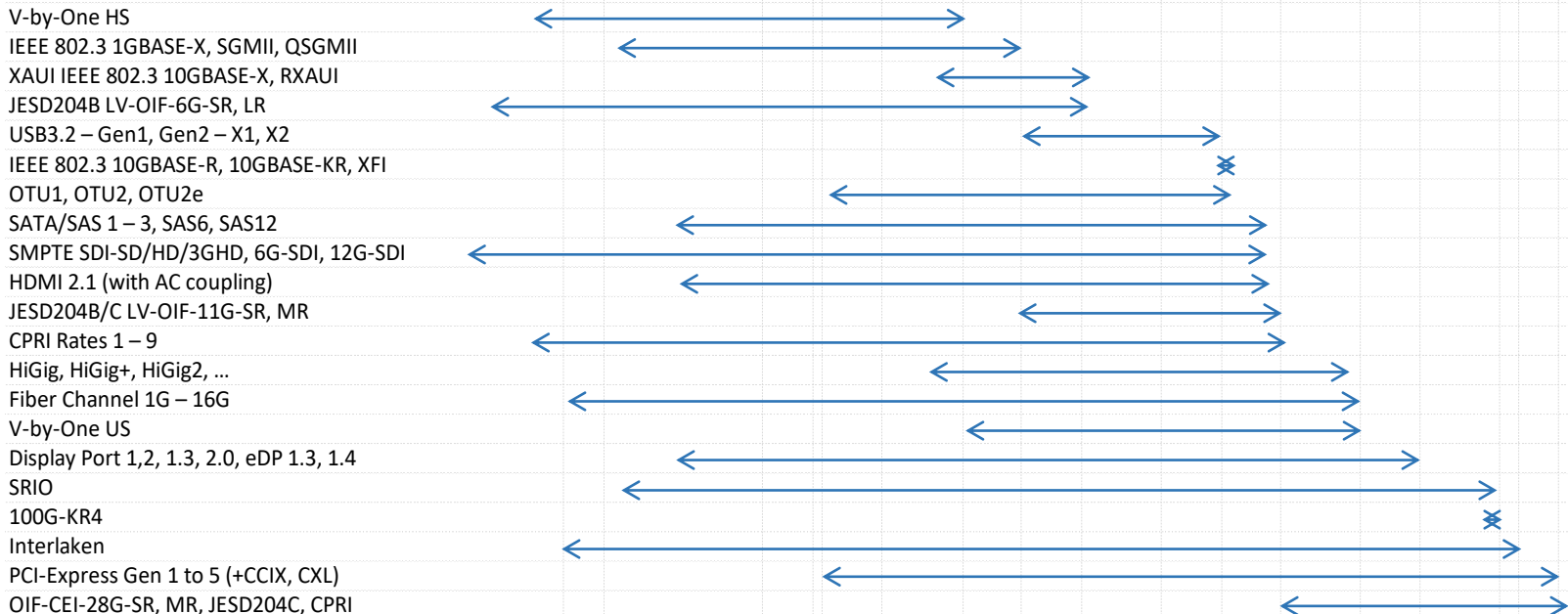
GF40LP
 TSMC 40 LP, 40G ✓
 UMC 28 HLP
 TSMC 28 HPC+
 TSMC 12FFC/16FFC ✓
 TSMC 6/7FF, GF12LP+



Processes from 40LP to 12FF and 6FF

Very wide, continuous data rate operation

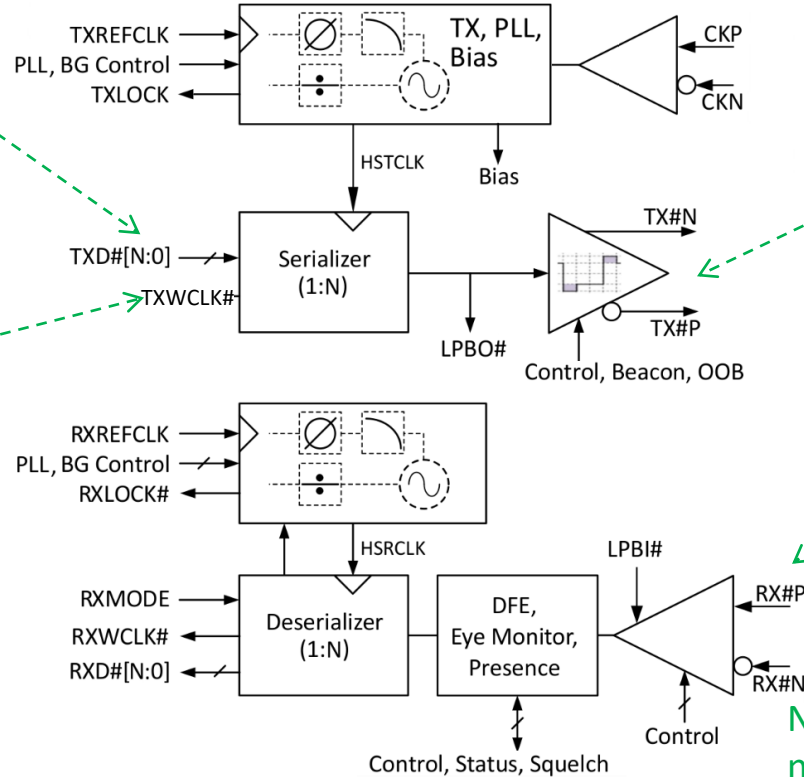
Supporting
 >20
 protocols
 Incl.
 10GbE,
 25GbE,
 PCIe3/4/5



Low-latency SerDes PMA

Ser/Des width can be custom
(E.g. 8b, 22b, to match MAC)

Programmable clock phase
for system latency reduction



Tx Load to 1st bit out
latency < 5UI
= 0.49ns @ 10.3Gbps

Rx last bit in to parallel
out latency < 8UI
= 0.77ns @ 10.3Gbps

Note : Latency specifications are
not STAC benchmarks

- License fee per Design Chip developed; win-win discounts for subsequent chips
- Accurate simulation models for system and latency verification
- Collaboration with ASIC design service companies fully supported
- License includes two years of unlimited support for SerDes/PLL IP integration into the chip, chip bring-up and debug
- Mark and return your Response Card for more information!