

# Hacking the Packet in ASIC with an eFPGA

STAC 2022

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**Achronix**  
Data Acceleration

- The only independent supplier of high-end FPGAs and eFPGA IP solutions
- Founded in 2004, profitable and strong financial position for IPO in 2023
- Headquarters in Santa Clara, CA

## Target Markets



Cloud / Data center  
AI/ML



Networking



Infrastructure



Test  
& Measurement



Automotive/  
ADAS



★ Financial ★  
Technology

**SPEEDSTER<sup>7t</sup>**

- 7nm Speedster7t FPGA Shipping
- VectorPath Accelerator Card Shipping

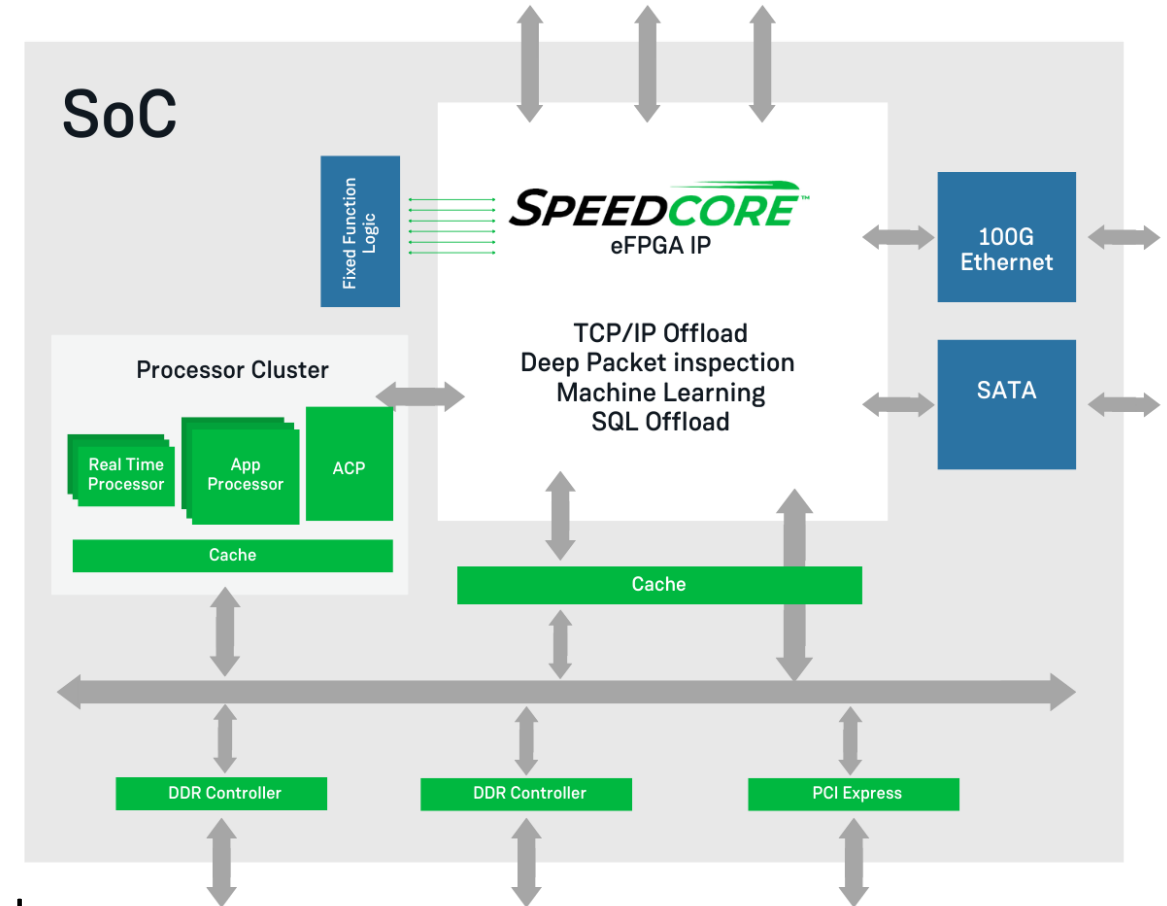
**SPEEDCORE™**

- Shipped > 15 million Speedcore eFPGA IP

**ACE**

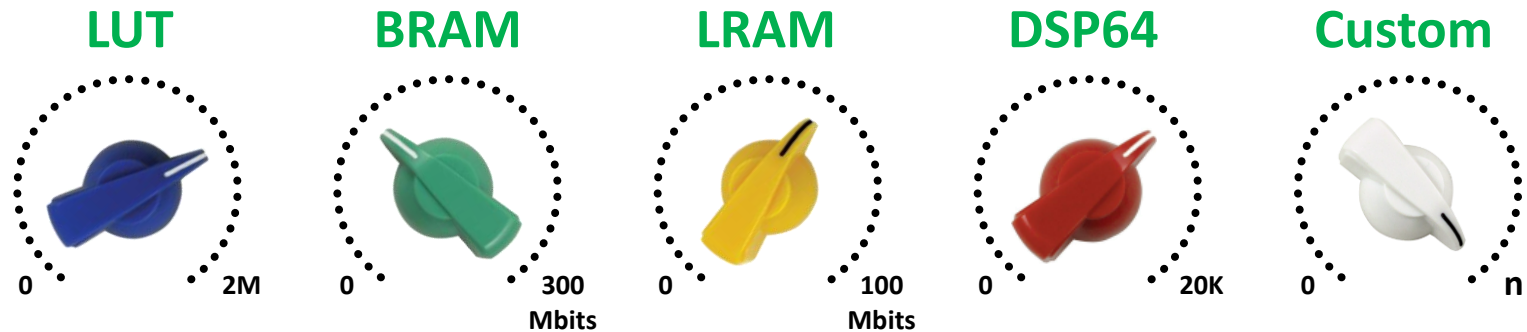
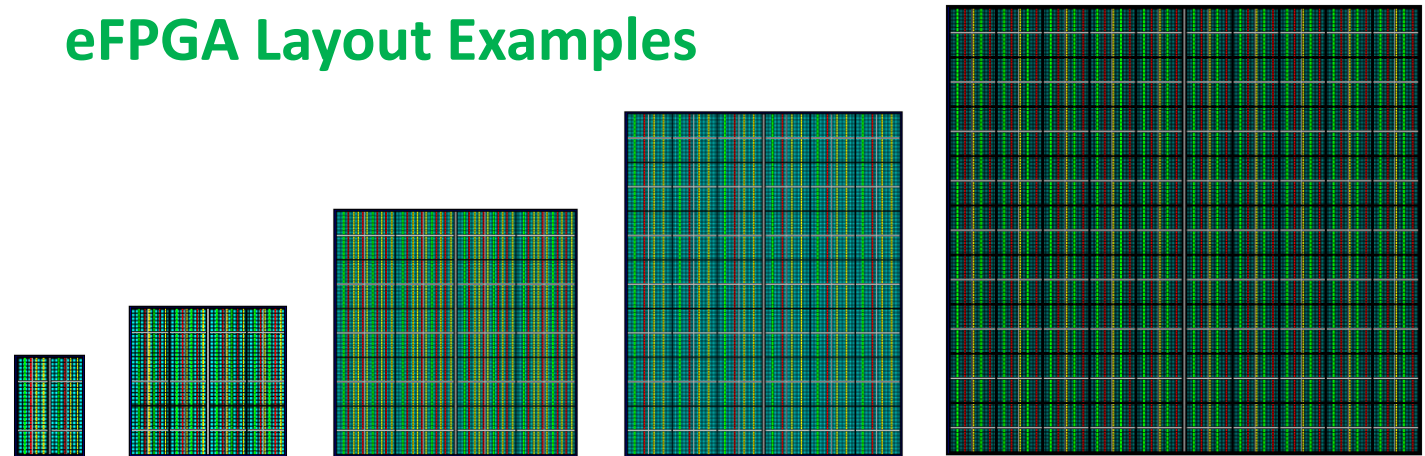
- Licensed to 600 companies
- 15+ years in development

- Speedcore eFPGA IP is a customized FPGA fabric for integration into an SoC or ASIC
- Customers define the amount of FPGA resources needed for their eFPGA implementation:
  - LUTs
  - Memory
  - DSP / MLP blocks
  - 2D NoC
- Available on TSMC 16FFC, 12FFC and N7 today
  - Able to port to any node at any foundry
  - Delivered in GDSII format
  - Supported with ACE development tools
- Achronix is the only supplier that offer eFPGA IP and FPGAs with over **15M eFPGA IP cores shipped**

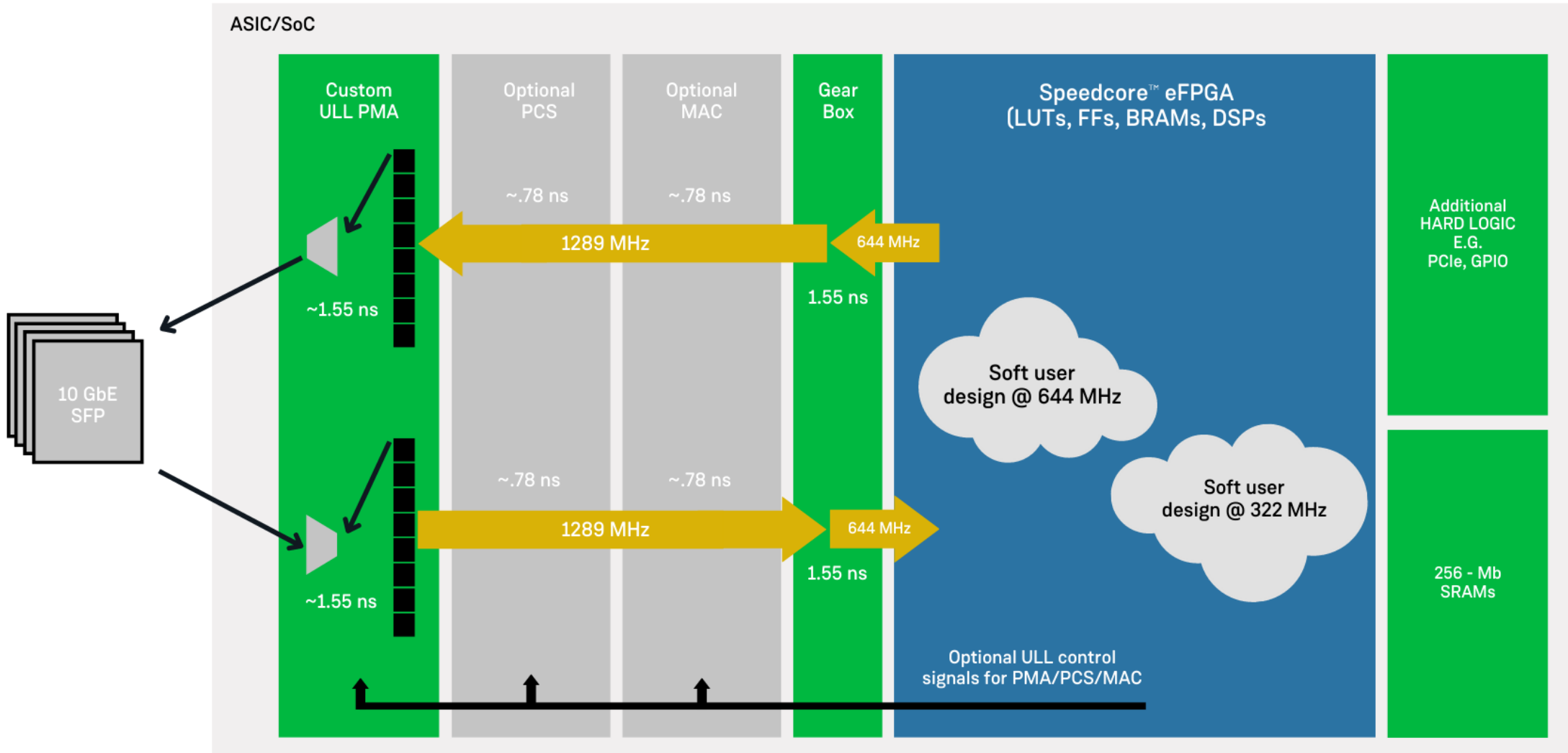


- Resources are designed as building block structures that can easily be combined to build any size eFPGA
- Custom eFPGA IP resource mix is defined by the customer
- IP delivered as physically laid out transistors for efficient ASIC integration

## eFPGA Layout Examples



# UDP-to-TCP Latency - Under 10 ns with Ultra-Low-Latency Data Path





Not STAC benchmarks


# Thank you

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Let's connect

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