Advanced Debugging For Your FPGAs and Algorithms

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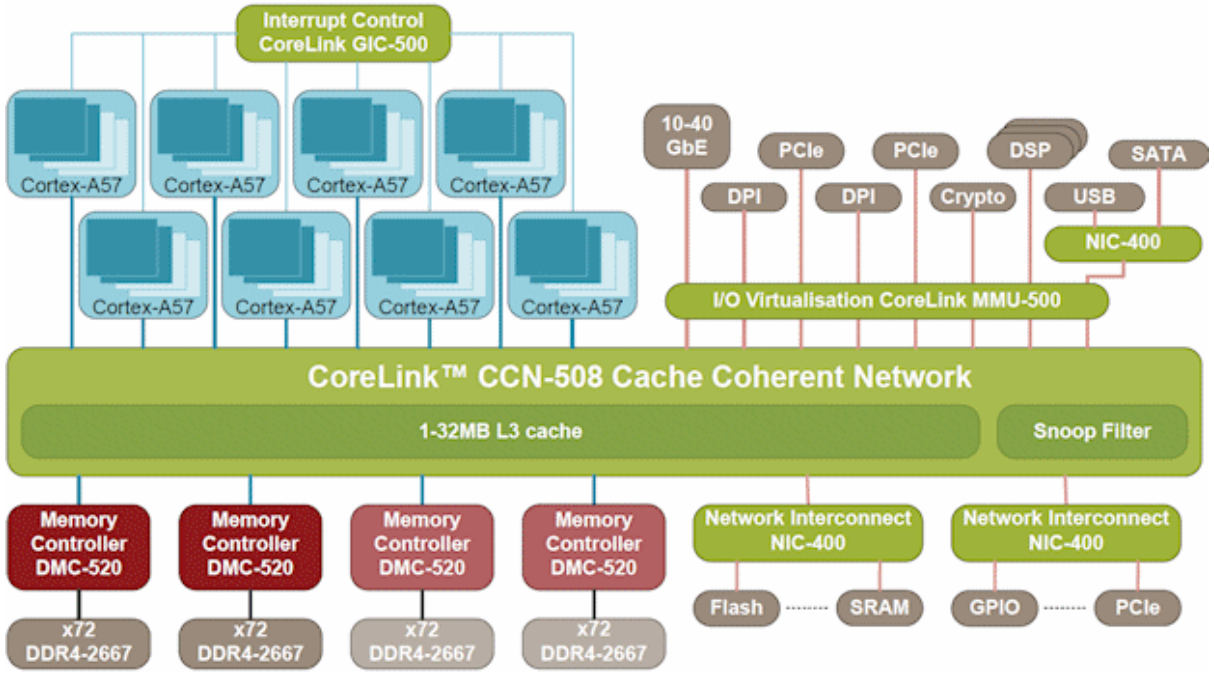
David Lidrbauch
Simulation Product Manager

Mentor®
A Siemens Business

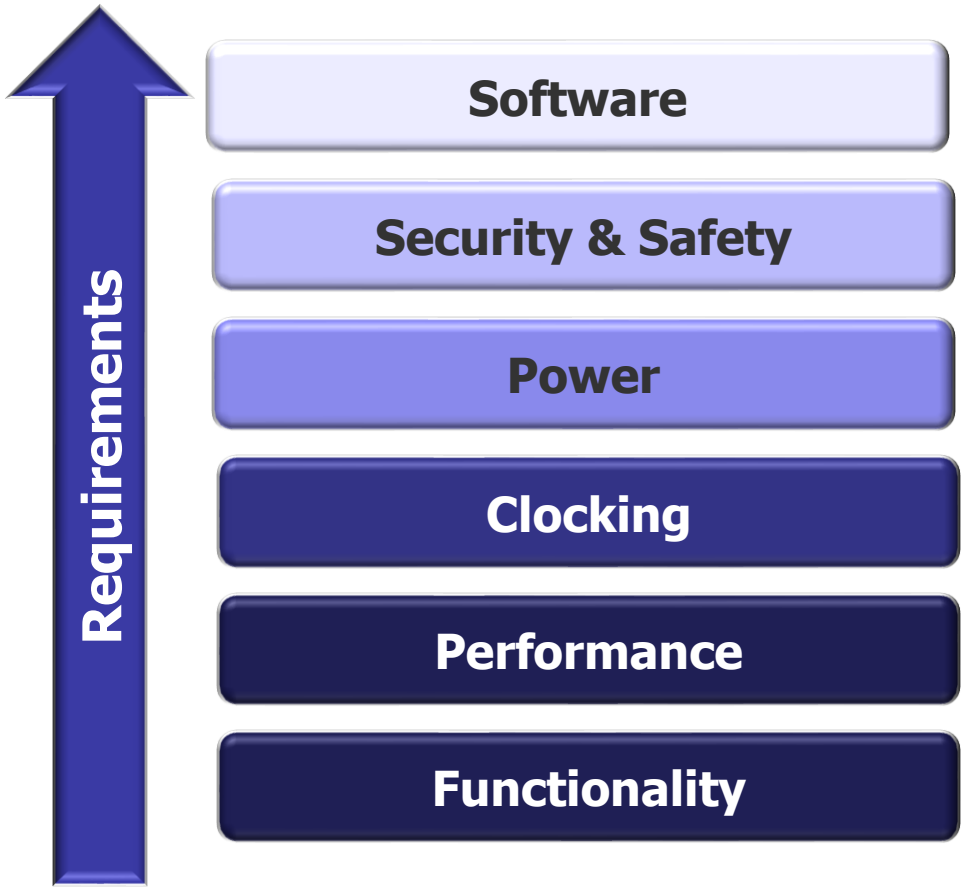
Verification Complexity

Emergence of New Layers of Verification Requirements & Need for Capacity/Performance



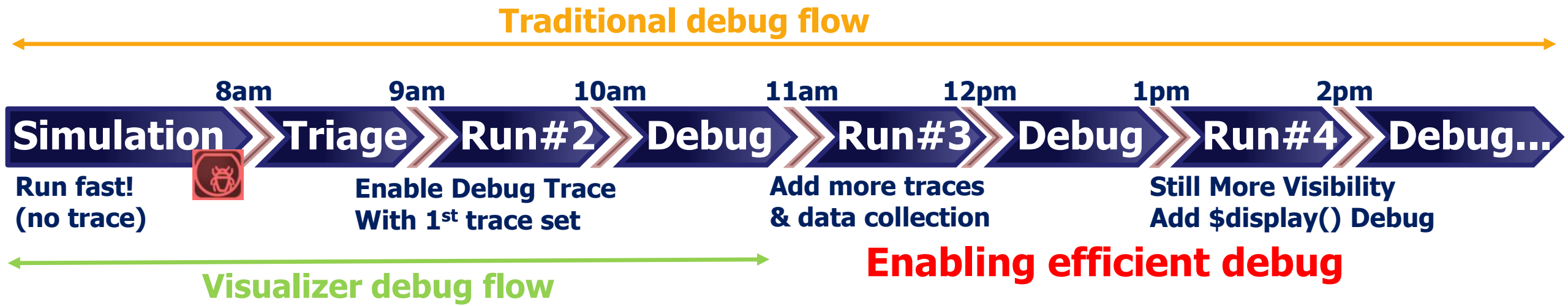
AMBA 5 CHI

https://techreport.com/review/26427/arm-lays-the-foundation-for-a-data-center-invasion



Full Design/TB Visibility by default

Reducing the latency of root-cause analysis

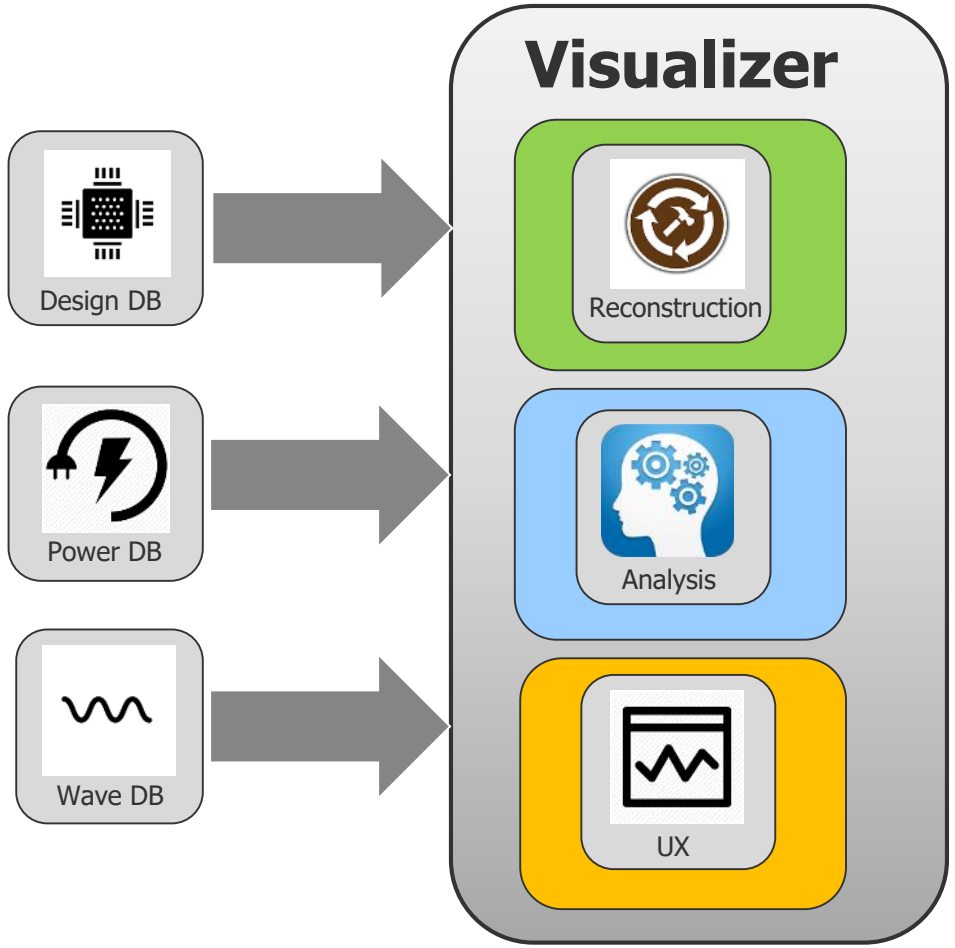


- Minimum trace set for fast simulation and compact results
- High performance "smart" reconstruction of signals
- Save Time by Capturing More Data, Faster, First Time

Questa Visualizer Debug

Context aware debug for complex heterogeneous verification environments

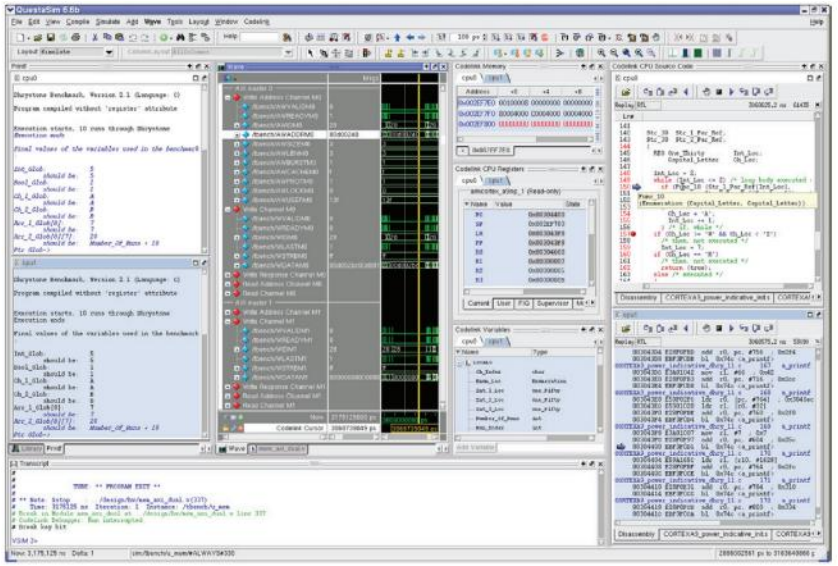
- Intelligent Debug
  - Single click root cause analysis
  - Heat maps to Visualizer data patterns
- Adaptive Environment
  - Domain aware - Power, UVM, SW… in a single cockpit
  - Same UX across all Engines
- Scalable Solution
  - Data Reconstruction for Compact DB
  - Loads 500m gate design in seconds



Questa Visualizer Debug – Multi-Domain Integration

Consistent User Interface And Context Aware Debug

- Codelink-Aware (Hardware + Software debug)
  - Interactive step forward and backward w/ Live and Replay
  - HW & SW integration (O, I, U, X states)
  - 100% cycle accurate SW source code + HW waveforms
- X-Tracing (Reset debug)
  - Resets crossing clock domains
  - Ambiguity testing of X-Pessimism/optimism
  - Source tracing of unknown state (X)
- Visibility (Higher level view)
  - Schematic, Finite State Machine, and Transactions
- UVM Testbench debug live and post-sim
- Veloce Emulation debug acceleration
  - Quickly find and solve extremely long application issues

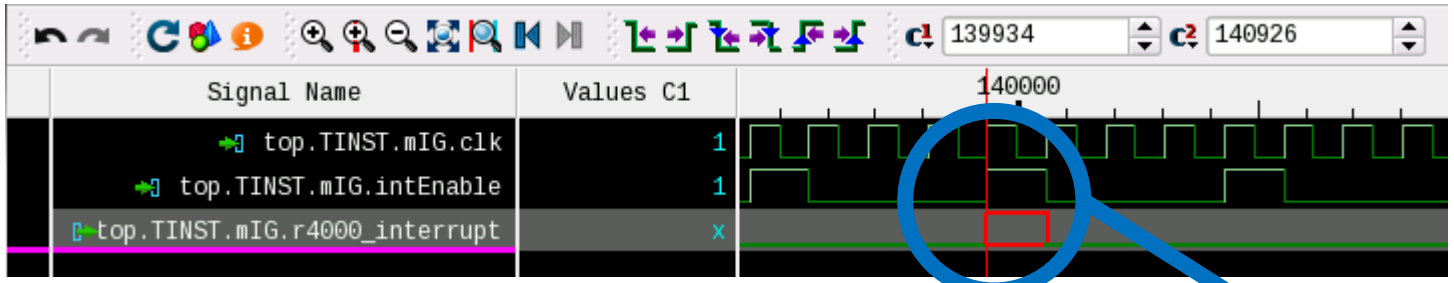


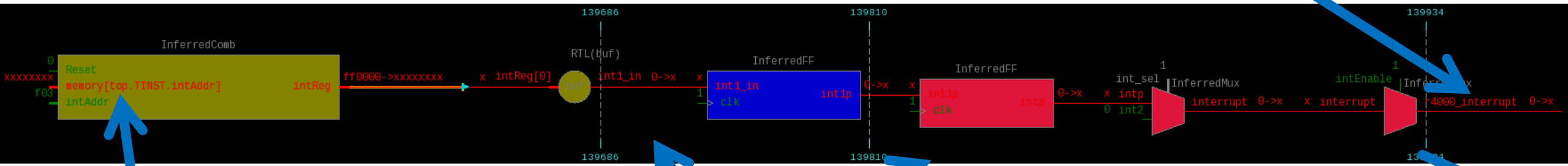
Questa® Codelink provides full processor(s) debug visibility for more efficient SoC debugging and verification.

Find Bug Root Cause Faster

Intuitive Temporal Causality Trace Back

X on Interrupt?





Causal Transition Identified

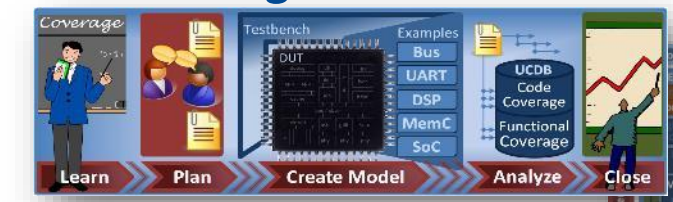
Automatic trace-back through combinational AND sequential elements to root cause Using wave, schematic & source views

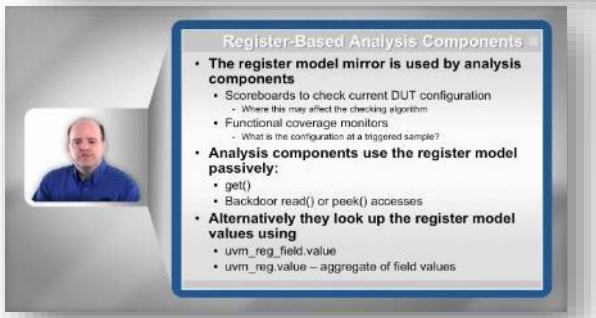
Questa Visualizer Debug and Verification

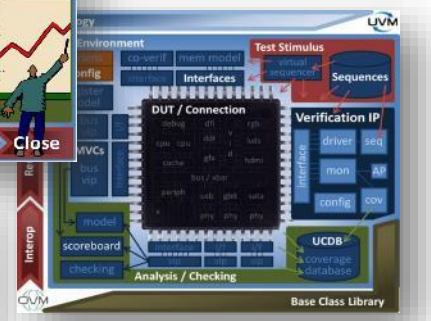
For More Information

- **Come to our booth for a demo**
  - How to shift left production and deployment
  - Efficient verification using simulation, formal tools, emulation, prototyping
  - Debug and coverage of FPGA designs including HW + SW verification
  - Advanced algorithm verification
- Verification Academy www.verificationacademy.com
  - Online Video Courses
  - Verification Cookbooks
  - Discussion Forums
  - Patterns Library
  - On Demand Seminars
- Mentor Web-page www.mentor.com/products/fv/visualizer-debug
  - Request a demo
  - Start an evaluation

Coverage Cookbook







UVM Cookbook

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